

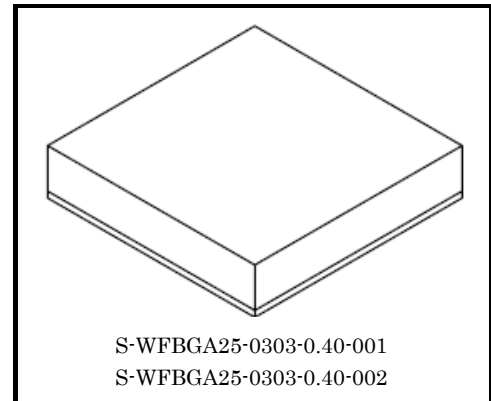
CDMOS Integrated Circuit Silicon Monolithic

# TC7710WBG

IC for Battery Charger

## 1. Outline

The TC7710WBG is a programmable battery charger for lithium-ion and lithium-polymer battery pack. The TC7710WBG supports charge current up to 2.0A. For handheld devices with high capacity battery pack, this IC can charge the battery more quickly compared to the conventional devices.



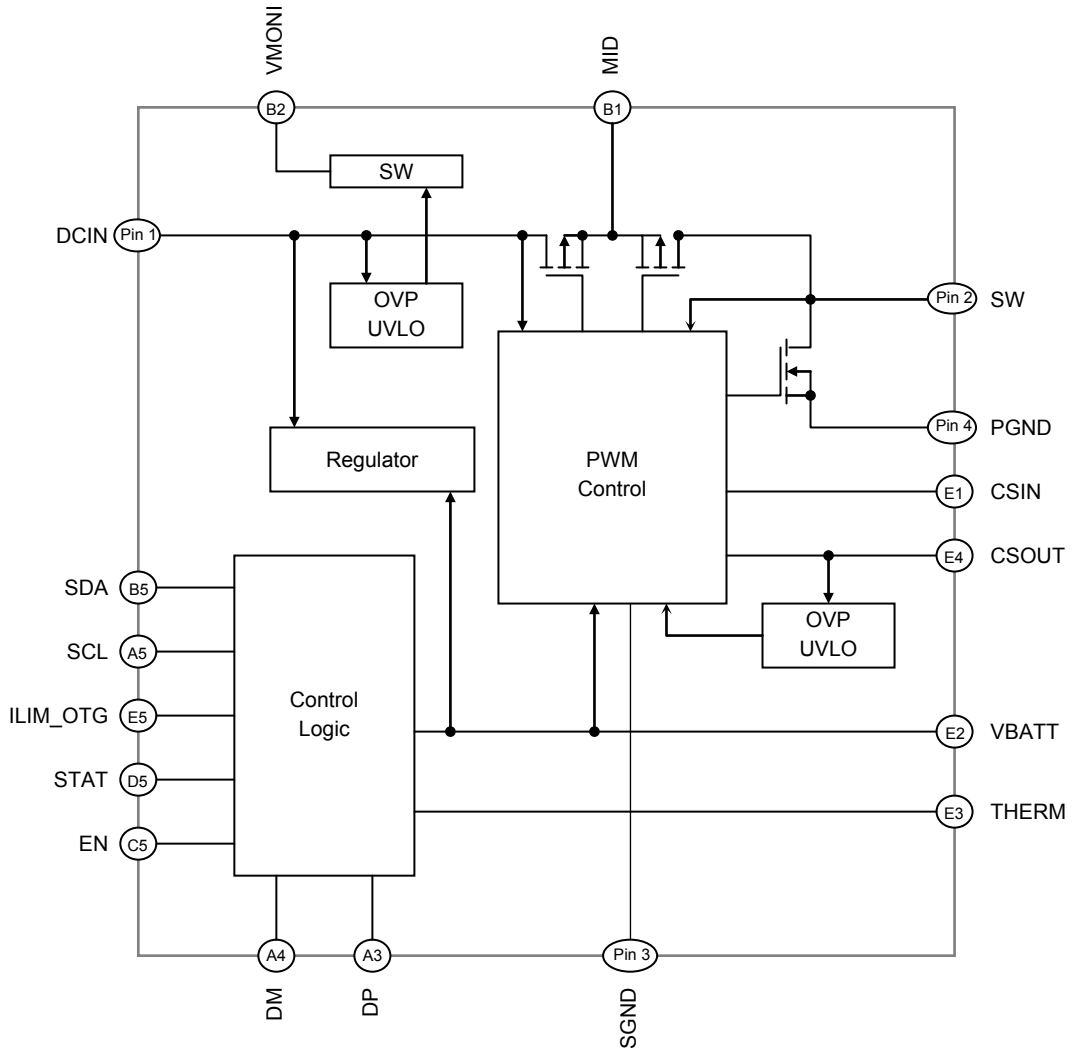
## 2. Applications

Mobile phones  
Devices with a single cell lithium-ion battery

## 3. Features

- Input voltage : 4.35V to 6.5V
- Battery Charging Specification 1.2 detection
- Battery shutdown current : 38 $\mu$ A(Typ.)
- Maximum charge current : 2.0A
- Protections and detections
  - Input over voltage protection (IOVP)
  - Under voltage lock out (UVLO)
  - Input current control
  - Battery voltage monitor
  - Battery temperature monitor
- Switching frequency : 3.0MHz
- Package : WCSP25 pin

**4. Block Diagram**



**Figure 4-1 Block Diagram**

Pin 1 : DCIN pin: A1 and A2.

Pin 2 : SW pin: C1 and C2.

Pin 3 : SGND pin: C3 and D3.

Pin 4 : PGND pin: D1 and D2.

Note. : Please refer to Application Circuit about parts and pin connection.

5. Pin Assignment

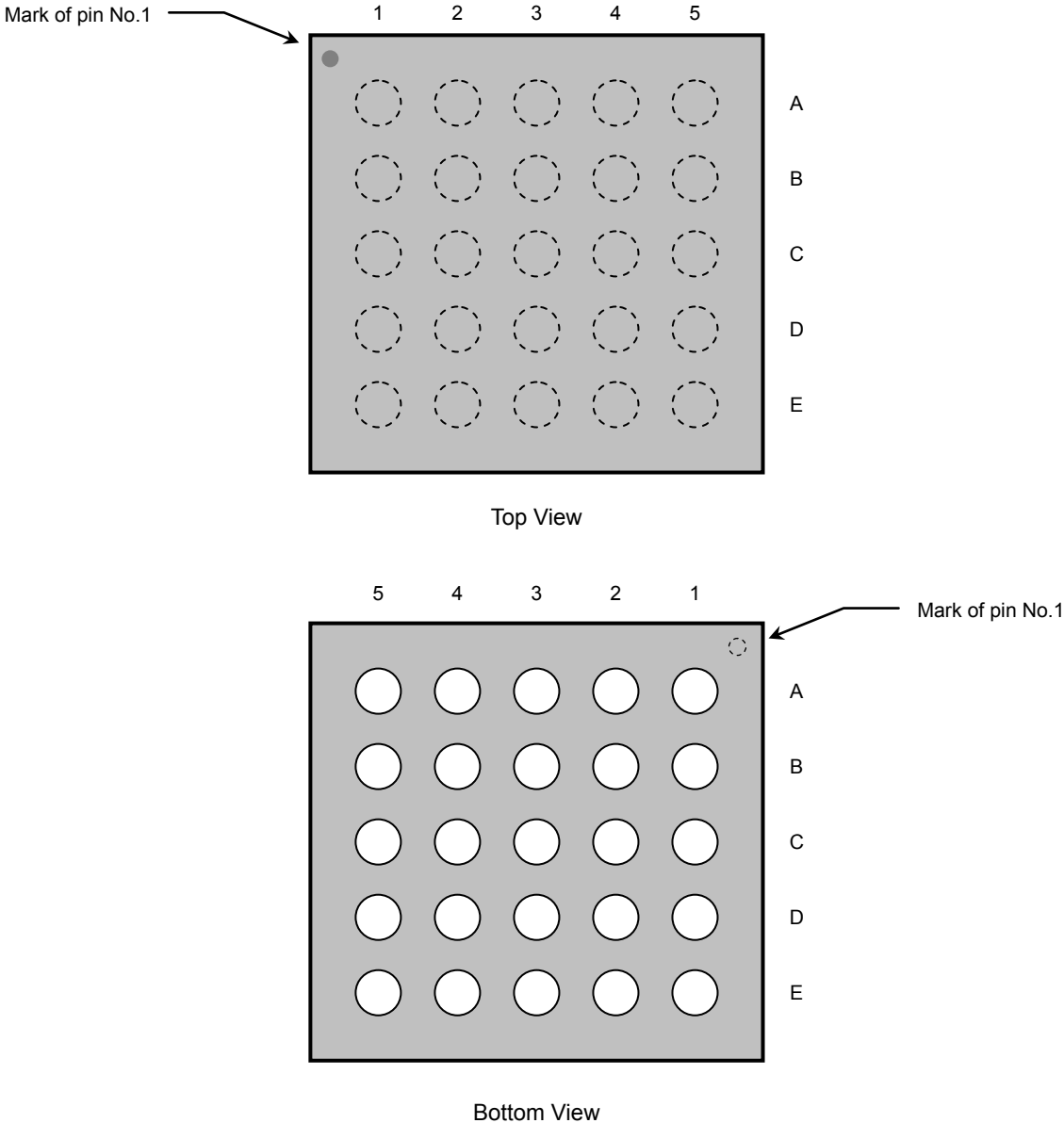


Figure 5-1 Pin Assignment

Note.: Please pay attention that corner pin which is next to the mark of No.1 is A1.

**6. Pin Functions**

**Table 6-1 Pin Functions (1)**

Pin No.	Pin name	I/O	Pin description											
A1, A2	DCIN	I/O	<p>I/O pin for USB VBUS / Input pin for AC adapter</p> <table border="1"> <tr> <td>Charge</td> <td>DC voltage input mode (+4.35V to +6.5V)</td> </tr> <tr> <td>OTG</td> <td>Voltage 5V output mode</td> </tr> </table> <p>The capacitor of 1.0<math>\mu</math>F or more must be connected between DCIN pin and GND to stabilize the voltage.</p>	Charge	DC voltage input mode (+4.35V to +6.5V)	OTG	Voltage 5V output mode							
Charge	DC voltage input mode (+4.35V to +6.5V)													
OTG	Voltage 5V output mode													
A3	DP	I/O	<p>I/O pin (+) for power source detection It is connected to D+ pin of the USB connector.</p>											
A4	DM	I/O	<p>I/O pin (-) for power source detection It is connected to D- pin of the USB connector.</p>											
A5	SCL	I	<p>Signal input pin for I<sup>2</sup>C bus clock Input pin of clock signal for serial communication. Pull-up resistance should be connected to SCL pin because it is an open-drain pin.</p>											
B1	MID	I	<p>FET midpoint input pin. Middle-point voltage pin of high side MOSFET. The capacitor of 2.2<math>\mu</math>F or more should be connected between MID pin and GND to stabilize the voltage.</p>											
B2	VMONI	O	<p>Input monitor for DC voltage The voltage corresponding to DCIN is outputted and monitored in the range of UVLO to OVLO.</p>											
B5	SDA	I/O	<p>I/O pin for I<sup>2</sup>C bus data signal. Pull-up resistance should be connected to SDA pin because it is an open-drain pin.</p>											
C1, C2	SW	O	<p>PWM signal output pin PWM signal output pin for DCDC convertor. One-side of the inductor is connected to this pin.</p>											
C3, D3	SGND	-	<p>Power supply pin for small signal (GND).</p>											
C5	EN	I	<p>Input pin for enable signal. This is a charge control pin for enable and resume. As for setting logic, polarity can be converted by register data.</p> <table border="1"> <thead> <tr> <th rowspan="2">ENPINPOL (11H, bit0)</th> <th colspan="2">EN signal</th> </tr> <tr> <th>Low</th> <th>High</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Charge</td> <td>Stop charge</td> </tr> <tr> <td>1</td> <td>Stop charge</td> <td>Charge</td> </tr> </tbody> </table> <p>Pay attention that validity of EN pin changes depending on ENSEL (11H, bit2).</p>	ENPINPOL (11H, bit0)	EN signal		Low	High	0	Charge	Stop charge	1	Stop charge	Charge
ENPINPOL (11H, bit0)	EN signal													
	Low	High												
0	Charge	Stop charge												
1	Stop charge	Charge												
D1, D2	PGND	-	<p>Power supply pin (GND) for large signal.</p>											
D5	STAT	O	<p>Status signal output pin Error and operation state set by register are outputted from STAT pin. When error is generated, the TC7710WBG outputs logic low. Pull-up resistance should be connected to STAT pin because it is an open-drain pin.</p>											

Table 6-2 Pin Functions (2)

Pin No.	Pin name	I/O	Pin description
E1	CSIN	I	Current sense input pin Connect high side of the current sense resistance.
E2	VBATT	I	Sub power supply / Kelvin sense input pin Connect + pin of battery directly.
E3	THERM	I	Battery thermistor sense input pin Temperature can be detected by connecting this pin to "T pin" of ordinary battery pack. Connect this pin to one-side of the thermistor (10 / 25 / 50 / 100kΩ NTC thermistor) which is inside of the battery pack or on the PCB.
E4	CSOUT	I/O	Current sense I/O pin Connect low side of the current sense resistance.
E5	ILIM_OTG	I	Input pin for control input current or Input pin for switching OTG operation This pin sets input current and switches OTG operation. Current level of charging mode is controlled (USB mode / AC mode) or Valid of invalid or OTG mode is switched.
B3, B4, C4, D4	TEST	-	IC test pin. TOSHIBA test pin. It must be open.

## 7. Functions

### 7.1 Input current limit

Input current from DCIN pin can be limited to the value set by ILIM\_OTG pin or I<sup>2</sup>C (Refer to the table below.). When input current exceeds the preset value, the TC7710WBG limits current to below the preset value automatically. When DCIN voltage turns into below the threshold voltage set by I<sup>2</sup>C, the TC7710WBG limits current to the USB100 level (Max 100mA) and indicates an interrupt signal. To resume the current limit to the former level, the interrupt signal must be cleared (Refer to the command: INTCLR5 (15H, bit5).). After clearing the interrupt signal, input current limit is set to the former level quickly. For safe use, input current limit is set to lower value and the interrupt signal can be cleared.

**Table 7-1 Command (1)**

Command	Register No./ bit No.	Contents
ACILMT4-0	03H,bit7-3	AC input current limit
USB51	13H,bit6	USB mode setting when ILIM_OTG is valid
ATPSDET	13H,bit4	Automatic power source detection
LMT_OTG1-0	13H,bit3-2	Input current limit setting
ILIMLVL1-0	13H,bit1-0	Input current limit setting when I <sup>2</sup> C is valid.
ATILMT	13H,bit5	Current limit function by DCIN voltage
INTATIL	20H,bit5	Generated the interrupt factor of input current limit

(1) Forced setting (13H,bit4="1")

Input current limit	Input current limit setting ILIM_OTG pin / I <sup>2</sup> C	Source detection DP / DM detection
USB500	USB500	*
USB100	USB100	*
AC	AC	*

(2) USB automatic detection setting (13H,bit4="0")

Input current limit	Input current limit setting ILIM_OTG pin / I <sup>2</sup> C	Source detection DP / DM detection
USB500	USB500	Unconnected
	USB500	DCP
USB100	USB100	Unconnected
	*	SDP
	*	CDP
AC	AC	*

Cautions: USB automatic detection setting

- In case input current limit setting is AC, source detection result is ignored.
- In case input current limit setting is USB500 and source detection is SDP or CDP, input current is limited 100mA.
- In case input current limit setting is USB100 and source detection is DCP, input current is limited 100mA.

DCP: Dedicated Charging Port

SDP: Standard Downstream Port

CDP: Charging Downstream Port

## 7.2 DCIN input voltage protection

When input voltage from DCIN pin exceeds specified voltage (Typ. 6.5V), input is shutdown. Charge is valid when input voltage is higher than the UVLO and lower than the OVLO. As soon as DCIN input supply is removed, charge is invalid automatically. Under the condition that charge is invalid, UVLO / OVLO detection for DCIN pin and OVLO detection for battery voltage are invalid.

## 7.3 Preliminary charge state

When DCIN input supply is connected, the TC7710WBG check the following items for charge start-up. After starting charge, charge is suspended when one of the following items is outside the limits

- (1) DCIN input voltage  $\geq$  UVLO voltage, DCIN input voltage  $\leq$  OVLO voltage
- (2) DCIN voltage > Battery voltage + 100mV
- (3) Charge is enabled. (Set by I<sup>2</sup>C or EN pin. Refer to the command: ENSEL(11H,bit2), ENCMD(11H,bit1), ENPINPOL(11H,bit0).)
- (4) Battery temperature is between high limit and low limit (Refer to the command: TEMPDET(12H,bit7), BIASCRT1-0(1EH,bit7-6), COLDVTH1-0(1EH,bit3-2), HOTVTH1-0(1EH,bit1-0)).

**Table 7-2 Command (2)**

Command	Register No./ bit No.	Contents
ENSEL	11H,bit2	EN control
ENCMD	11H,bit1	EN control by I <sup>2</sup> C
ENPINPOL	11H,bit0	Polarity of EN pin
TEMPDET	12H,bit7	Battery temperature detection

## 7.4 Trickle charge

Preliminary charge state is OK, the TC7710WBG starts trickle charge with 50mA (Typ.) if battery voltage is lower than 2.1V.

## 7.5 Pre-charge

When battery voltage exceeds 2.1V, the TC7710WBG starts pre-charge with the charge current set by the register. Pre-charge continues until the battery voltage reaches the fast charge threshold voltage set by the register (Refer to the command: CCVTH2-0(01H,bit2-0)). If the battery voltage is not exceed the fast charge threshold voltage before the pre-charge timer expires, charge is suspended and an interrupt signal is indicated (Refer to the command: INTCHGER(20H,bit1), ST\_TMER1-0(23H,bit1-0)). If battery voltage is lower to the trickle charge level during pre-charge, the TC7710WBG becomes trickle charge mode and indicates an interrupt signal (Refer to the command: INTVBAT(20H,bit6)). In this case, if trickle charge is invalid (12H,bit0= "1"), the TC7710WBG doesn't become trickle charge and doesn't indicate an interrupt signal.

**Table 7-3 Command (3)**

Command	Register No./ bit No.	Contents
PCI1-0	00H,bit1-0	Pre-charge current
CCVTH2-0	01H,bit2-0	Threshold voltage for fast charge

### 7.6 Fast charge (Constant Current charge mode)

When fast charge mode is valid, the TC7710WBG starts constant current charge mode if battery voltage exceeds the fast charge threshold voltage set by the register. The TC7710WBG limits charge current to below input current limit value (Refer to the command: CCISSET(12H,bit2), PRCCTH(12H,bit1), CCVTH2-0 (01H,bit2-0)). If battery voltage is lower to the pre charge level during fast charge, the TC7710WBG becomes pre-charge mode and indicates an interrupt signal (Refer to the command: INTVBAT(20H,bit6)).

**Table 7-4 Command (4)**

Command	Register No./ bit No.	Contents
CCI4-0	01H,bit7-3	Fast charge current
CCISSET	12H,bit2	Fast charge mode setting

### 7.7 Fast charge (Constant Voltage charge mode)

The TC7710WBG starts constant voltage charge mode if battery voltage becomes the float voltage set by the register during constant current charge mode (Refer to the command: FLTV6-0(02H,bit6-0)).

**Table 7-5 Command (5)**

Command	Register No./ bit No.	Contents
FLTV6-0	02H,bit6-0	Float voltage

### 7.8 Charge completion

When charge completion is valid (Refer to the command: CT(12H,bit3)), charging is completed if charge current is lower than the charge termination current set by the register (Refer to the command: CEI1-0(00H,bit5-4)). If charge timer has expired until charge is completed, the TC7710WBG terminates the charge and indicates an interrupt signal (Refer to the command: INTCHGER(20H,bit1), ST\_TMER1-0(23H,bit1-0)). If charge completion is invalid (CT(12H,bit3)=1), the TC7710WBG continues CV charge and doesn't indicate an interrupt signal. In this case, the TC7710WBG is controlled by I<sup>2</sup>C to terminate the charge. The status ST\_CGED0 (24H,bit4) can be checked if charge current is lower than the current set by the register during CV charge mode.

**Table 7-6 Command (6)**

Command	Register No./ bit No.	Contents
CT	12H,bit3	Charge completion
CEI1-0	00H,bit5-4	Charge termination current
ST_CGED0	24H,bit4	Charge current is lower than the charge termination current (only CV mode).

### 7.9 Re-charge

The TC7710WBG recharges the battery when the battery voltage falls by a value set by the register below the float voltage (Refer to the command: FLTV6-0(02H,bit6-0), ATRCHGTH(00H,bit6) is fixed to 140mV. ). The TC7710WBG can recharge only when DCIN input supply is connected, charge is enabled and the charge start-up condition is satisfied before charge. In this case, the TC7710WBG is controlled by command to recharge the battery automatically (Refer to the command: ATRCHG(12H,bit4)).

**Table 7-7 Command (7)**

Command	Register No./ bit No.	Contents
ATRCHGTH	00H,bit6	Threshold voltage for automatic recharge. *140mV only.
ATRCHG	12H,bit4	Automatic recharge



### 7.10 Automatic charge

The TC7710WBG can start charge automatically regardless of enable control (Refer to the command: DBATVDET(00H,bit7), ATCHG(11H,bit3).) when battery voltage is lower than dead battery threshold. In case the battery voltage is higher than dead battery threshold, charge is controlled by EN pin / I<sup>2</sup>C, and in case the battery voltage is lower than dead battery threshold, the TC7710WBG starts charge when DCIN input supply is connected, charge is enabled and the charge start-up condition is satisfied before charge. A charge enable shall be set after 3ms since the float voltage is set. The TC7710WBG continues charge until charge is completed or pre-charge safety timer of 36minutes is expired.

**Table 7-8 Command (8)**

Command	Register No./ bit No.	Contents
DBATVDET	00H,bit7	Threshold for dead battery
ATCHG	11H,bit3	Automatic charge

### 7.11 USB OTG

The TC7710WBG can supply a regulated 5V output at the DCIN pin for powering peripherals compliant with the USB OTG specification (Refer to the command: OTGVCTL1-0(04H,bit5-4).). When only a battery is connected (AC adaptor or USB isn't connected) and battery voltage is higher than battery UVLO voltage, OTG control can be enabled by ILIM\_OTG pin or I<sup>2</sup>C (Refer to the command: OTGUVTH1-0(04H,bit1-0), OTGMD(13H,bit7), LMT\_OTG1-0(13H,bit3-2).). If battery UVLO, battery current limit and DCIN UVLO are occurred during OTG mode, OTG operation is suspended. OTG operation resumes by ILIM\_OTG pin or I<sup>2</sup>C. During OTG operation, output current is controlled by a value set by the register (Refer to the command: CCI4-0(01H,bit7-3).).When output current exceeds the preset value, the TC7710WBG shuts off the OTG voltage and indicates an interrupt signal (Refer to the command: INTOTGER(20H,bit3), ST\_OTGLM(22H,bit1).). When the chip temperature exceeds 135°C during OTG operation, the TC7710WBG shuts off the OTG voltage and indicates an interrupt signal (Refer to the command: INTOTGER(20H,bit3), ST\_OTGJCT(22H,bit3).). During OTG operation, a watchdog timer should be valid for system safety. When a watchdog timer is expired, the TC7710WBG shuts off the OTG voltage and indicates an interrupt signal (Refer to the command: OTGWDTM(10H,bit4), INTOTGER(20H,bit3), ST\_OTWDT(22H,bit2).).

**Table 7-9 Command (9)**

Command	Register No./ bit No.	Contents
CCI4-0	01H,bit7-3	OTG battery current limit
OTGVCTL1-0	04H,bit5-4	OTG output voltage
OTGUVTH1-0	04H,bit1-0	Battery UVLO setting in OTG
OTGWDTM	10H,bit4	OTG watchdog timer
OTGMD	13H,bit7	OTG control by I <sup>2</sup> C
LMT_OTG1-0	13H,bit3-2	OTG control setting

### 7.12 Watchdog timer

A watchdog timer is reset with every I<sup>2</sup>C ACK signal transmitted from a system. If watchdog timer is expired during the charging / OTG operation, the TC7710WBG suspends the charging / OTG operation, indicates an interrupt signal and reset the following registers: 00H-13H, 1EH, and 1FH (e-Fuse data is reloaded.). During OTG operation, a watchdog timer should be valid for system safety. And standby watchdog timer should be valid when the TC7710WBG doesn't charge or supply OTG power (Refer to the command: STBWDTM(10H,bit5), OTGWDTM(10H,bit4), CHGWDTM(10H,bit3)). However both watchdog timers are not valid from a fully charged state to an automatic recharge starts, since the TC7710WBG isn't in a charge mode or a standby mode. To set a charge disable, standby watchdog timer is valid for this time.

**Table 7-10 Command (10)**

Command	Register No./ bit No.	Contents
OTGWDTM	10H,bit4	OTG watchdog timer
CHGWDTM	10H,bit3	Charge watchdog timer
STBWDTM	10H,bit5	Standby watchdog timer

### 7.13 Safety timer

The TC7710WBG has a pre-charge timer of 36 minutes and a charge timer of 240 minutes (Refer to the command: PRCHGTM(10H,bit2), CHGSTM(10H,bit1)). A pre-charge timer of 36 minutes is started after preliminary charge state is OK, the TC7710WBG starts trickle charge. And this timer is reset when the mode is changed from pre-charge to fast charge. A charge timer of 240 minutes is also started after preliminary charge state is OK, the TC7710WBG suspends the charging if charge current isn't lower than the charge termination current within a timer. It is possible not to include trickle charge time in the charge timers (Refer to the command: TCSTON(10H,bit0)). Both timers can be cleared by I<sup>2</sup>C in case charge timers are monitored by system (Refer to the command: CHGTMCLR(10H,bit6)). When the TC7710WBG starts recharge in case an auto recharge is valid, these safety timers aren't valid. Therefore it is recommended that an external timer is applied by system for charge protection.

**Table 7-11 Command (11)**

Command	Register No./ bit No.	Contents
PRCHGTM	10H,bit2	Pre-charge timer
CHGSTM	10H,bit1	Charge timer
TCSTON	10H,bit0	Include or not include trickle charge time in the timers
CHGTMCLR	10H,bit6	Timer clear

### 7.14 Operating state

STAT pin is output that indicates operating state. When battery is charging or DCIN voltage is lower than UVLO / higher than OVLO, this pin is asserted low level. A type of state from STAT pin is controlled by command, and the output is invalidated controlled by command (Refer to the command: STATMD(14H,bit2), STATOUT(14H,bit1)). STAT pin is open-drain output, a pull-up resistor should be connected to this pin.

**Table 7-12 Command (12)**

Command	Register No./ bit No.	Contents
STATMD	14H,bit2	Select a type of state from STAT pin
STATOUT	14H,bit1	STAT output ON/OFF

### 7.15 Interrupt / Abnormal detection

STAT pin is output that indicates seven interrupt signals. Interrupt signal and interrupt mask are set by I<sup>2</sup>C. The TC7710WBG outputs a pulse signal from STAT pin for 0.8ms every 350ms and indicates an interrupt signal to system. The system checks an interrupt factor, clears the factor and executes the interrupt process according to the factor.

Standby WDT error  
 OTG error  
 Re-charge  
 Charge error  
 Charge completion  
 Occurrence of automatic input current limit  
 Occurrence of charge state back to previous mode

The following tables describe the error recovery.

**Table 7-13 Interrupt process**

#### Standby WDT error

Interrupt factor	TC7710WBG process	Recovery process
Timer expired	Registers of 00H-13H, 1EH, and 1FH are initialized. Standby mode transition	Set registers of 00H-13H, 1EH, and 1FH.

#### OTG error

Interrupt factor	TC7710WBG process	Recovery process
WD Timer expired	Shut off OTG supply. Registers of 00H-13H, 1EH, and 1FH are initialized. Standby mode transition	Set registers of 00H-13H, 1EH, and 1FH.
Exceed current limit	Shut off OTG supply.	Control OTG function disable to enable manually.
Battery UVLO occur	Shut off OTG supply.	Control OTG function disable to enable manually.
Exceed chip temperature	Shut off OTG supply.	Control OTG function disable to enable manually.
Output (DCIN) voltage drop under UVLO	Shut off OTG supply.	Control OTG function disable to enable manually.

#### Re-charge

Interrupt factor	TC7710WBG process	Recovery process
Vbat < Vfloat - 140mV	Restart charging (ATRCHG=0)	-

## Charge error

Interrupt factor	TC7710WBG process	Recovery process
Input OVLO occur	Stop charging.	After charge start-up condition is satisfied, the TC7710WBG restarts charging from standby mode.
Input UVLO occur	Stop charging.	After charge start-up condition is satisfied, the TC7710WBG restarts charging from standby mode. * The TC7710WBG doesn't output an interrupt signal since all registers are initialized for POR.
DCIN < Vbat + 105mV	Stop charging.	After charge start-up condition is satisfied, the TC7710WBG restarts charging from standby mode.
Out of battery temperature limit	Continue charging. (TEMPDET="0")	EN should be turned off manually.
	Suspend charging. (TEMPDET="1")	After charge start-up condition is satisfied, the TC7710WBG resumes charging automatically.
Exceed chip temperature	Continue charging. (OVTLMT="0")	EN should be turned off manually. * It is recommended charging is suspended in this case (OVTLMT(12h,bit6)=1).
	Suspend charging. (OVTLMT="1")	After charge start-up condition is satisfied, the TC7710WBG resumes charging automatically.
Battery OVLO occur	Stop charging. (BATOV="1")	After charge start-up condition is satisfied, EN should be turned on manually.
Unconnected battery	Stop charging.	After charge start-up condition is satisfied, EN should be turned on manually.
Charge WDT expired	Continue charging. Registers of 00H-13H, 1EH, and 1FH are initialized.	Set registers of 00H-13H, 1EH, and 1FH. * Charge timers are running on.
Charge timer expired	Stop charging.	EN should be turned on manually.
Input voltage drop	Continue charging. The TC7710WBG limits current to the 100mA. (ATILMT="0")	To resume the current limit to the former level, the interrupt signal must be cleared.

## Charge completion

Interrupt factor	TC7710WBG process	Recovery process
Ichg < Iterm	Charge completion (CT="0")	-

## Occurrence of automatic input current limit

Interrupt factor	TC7710WBG process	Recovery process
Exceed input current	Continue charging. The TC7710WBG limits current to the 100mA.	To resume the current limit to the former level, the interrupt signal must be cleared.

## Occurrence of charge state back to previous mode

Interrupt factor	TC7710WBG process	Recovery process
Charge state is back to previous mode by battery voltage drop.	-	-

**Table 7-14 Command (13)**

Command	Register No./ bit No.	Contents
INTOUT	14H,bit3	Select an information from STAT pin.
STATOUT	14H,bit1	Control an output from STAT pin.
INT***	20H,bit6-0	Interrupt factor
ST_***	21H, 22H, 23H	Status information

### 7.16 Chip temperature monitoring

Chip temperature is monitored during charge/OTG. When chip temperature exceeds 135°C, chip temperature monitoring bit is set high. And when chip temperature falls 115°C, it is set low (Refer to the command: ST\_JCTON(21H,bit2)). Charge stops when chip temperature monitoring bit is set high. And charge re-starts automatically when it is set low. (It depends on the set conditions. Refer to the command: OVTLMT(12H,bit6).) OTG stops when chip temperature monitoring bit is set high (Refer to the command: ST\_OTGJCT(22H,bit3)).

**Table 7-15 Command (14)**

Command	Register No./ bit No.	Contents
ST_JCTON	21H,bit2	Chip temperature state (Charging mode)
ST_OTGJCT	22H,bit3	Chip temperature state (OTG mode)
OVTLMT	12H,bit6	Charge stop in high temperature

### 7.17 Battery temperature monitoring

Battery temperature is monitored before charging and in charging through THERM pin. When battery temperature exceeds the programmed temperature limit, charge can be suspended (Refer to the command: TEMPDET(12H,bit7)). While battery temperature is out of the limit range, the TC7710WBG stops charge timer indicates charge error interrupt signal (Refer to the command: INTCHGER(20H,bit1), ST\_BATHT(21H,bit1), ST\_BATCL(21H,bit0)). And when the temperature becomes within the limit range, the TC7710WBG resumes charge and charge timer. As detection range is different depending on a characteristic of NTC thermistor, external resistance which is the same value of R25 is connected in parallel typically. And the intended range of temperature is set (Refer to the command: COLDVTH1-0(1EH,bit3-2), HOTVTH1-0(1EH,bit1-0)). The TC7710WBG supports thermistors which value of R25 is 10k $\Omega$ , 25k $\Omega$ , 50k $\Omega$ , and 100k $\Omega$ . A current source of 200 $\mu$ A, 80 $\mu$ A, 40 $\mu$ A, and 20 $\mu$ A is selected depending on the resistor (Refer to the command: BIASCRT1-0(1EH,bit7-6)).

**Table 7-16 Temperature limit**

Vtherm [V]	$\beta$								
	3000	3250	3500	3750	4000	4250	4500	4750	5000
0.509	61	58	55	53	51	50	48	47	46
0.574	55	53	50	49	47	46	45	44	43
0.647	49	47	45	44	43	42	41	40	39
0.726	43	42	40	39	39	38	37	36	36
1.000	25	25	25	25	25	25	25	25	25
1.399	1	3	5	6	7	8	9	9	10
1.491	-4	-2	0	1	2	4	5	6	7
1.577	-10	-8	-5	-4	-2	-1	1	2	3
1.654	-16	-13	-10	-8	-7	-5	-3	-2	-1

**Table 7-17 Command (15)**

Command	Register No./ bit No.	Contents
TEMPDET	12H,bit7	Charge control with battery temperature monitoring
BIASCRT1-0	1EH,bit7-6	Current source value for temperature monitoring
COLDVTH1-0	1EH,bit3-2	Threshold voltage for low temperature detection
HOTVTH1-0	1EH,bit1-0	Threshold voltage for high temperature detection
INTCHGER	20H,bit1	Charge error interrupt
ST_BATHT	21H,bit1	Battery high temperature detection status
ST_BATCL	21H,bit0	Battery low temperature detection status

### 7.18 Power source detection

The TC7710WBG corresponds to Battery Charging Specification Rev1.2. Automatic power source detection can be set by the register (Refer to the command: ATPSDET(13H,bit4)). Source detection starts as soon as DCIN is connected. There are four kinds of detection results as follows; non-connection, SDP (Standard Downstream Port), CDP (Charging Downstream Port), and DCP (Dedicated Charging Port) (Refer to the command: ST\_STYP1-0 (25H,bit1-0)). Input current limit can be set depending on the detection state (Refer to 7.1 Input current limit.).

**Table 7-18 Command (16)**

Command	Register No./ bit No.	Contents
ATPSDET	13H,bit4	Automatic power source detection
ST_STYP1-0	25H,bit1-0	Source detection result

### 7.19 Unconnected battery detection

The TC7710WBG executes battery detection through VBATT pin (Refer to the command: BATMSDET(11H,bit4)). When battery voltage is lower than 2.1V, the TC7710WBG starts trickle charge. And when battery voltage exceeds 2.1V, the TC7710WBG starts pre-charge. If battery voltage exceeds 3.3V within 85ms after starting pre-charge, the TC7710WBG detects as unconnected battery (Refer to the command: INTCHGER(20H,bit1), ST\_BATMS(21H,bit7)).

**Table 7-19 Command (17)**

Command	Register No./ bit No.	Contents
BATMSDET	11H,bit4	Execute battery detection
INTCHGER	20H,bit1	Charge error interrupt
ST_BATMS	21H,bit7	Unconnected battery detection

### 7.20 VMONI output

The TC7710WBG outputs the signal which monitored DCIN input voltage.

**Table 7-20 Command (18)**

Command	Register No./ bit No.	Contents
VMONICNT	14H,bit4	Output VMONI signal

7.21 Battery save mode

The TC7710WBG becomes battery save mode when DCIN is in UVLO and standby WDT is invalid, or when OTG is disable. If there are I<sup>2</sup>C signals among the battery save mode, the TC7710WBG changes the mode to the standby mode. Wait time 1ms is necessary to write next I<sup>2</sup>C signal successively. If there is a DCIN input among the battery save mode, the TC7710WBG enables POR and becomes standby mode.

7.22 I<sup>2</sup>C Bus

A communication between the TC7710WBG and the host is operated using I<sup>2</sup>C format. Both the clock line (SCL) and the data line (SDA) provide a communication between the TC7710WBG and the host. There are Start Condition and Stop Condition, when they send and receive the data. The commands are sent between Start Condition and Stop Condition. Refer to the following figure.

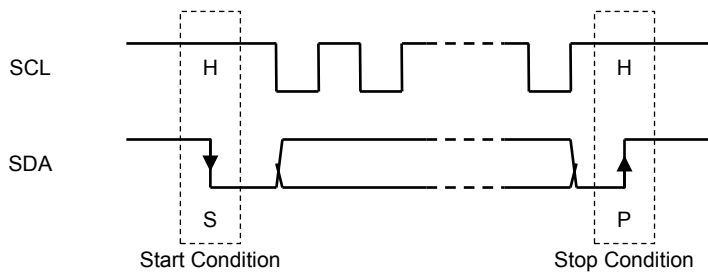


Figure 7-1 Relation between Start Condition and Stop Condition

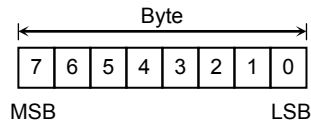
Table 7-21 List of the protocol symbols

Symbols	Descriptions
<b>S</b>	Start Condition
<b>SR</b>	Repeat Start Condition
<b>P</b>	Stop Condition
<b>Slave Address</b>	Slave Address(high 7 bits)
<b>R</b>	Read mode(TC7710WBG -> HOST)
<b>W</b>	Write mode(HOST -> TC7710WBG)
<b>X</b>	Undefined (1 or 0)
<b>A</b> / <b>A</b>	ACK (HOST -> TC7710WBG). This symbol in gray shows that the TC7710WBG output “Low” level when it receives ACK (TC7710WBG -> HOST)
<b>NA</b> / <b>NA</b>	NACK (HOST -> TC7710WBG). This symbol in gray shows that the TC7710WBG output Hi-Z when it receives NACK(TC7710WBG -> HOST)
<b>COMMAND CODE</b>	Command register for the TC7710WBG
<b>Data Byte</b>	This symbol shows 1 byte. This symbol in gray shows data flow from the TC7710WBG to HOST in read.
<b>Data Byte</b>	
...	This symbol shows that the block (bit or byte, Packet) is continued.



**7.22.1 Detailed bits**

The TC7710WBG supports the following I<sup>2</sup>C bus bit sequence.



**Figure 7-2 bit sequence**

**7.22.2 Start Condition / Stop Condition**

The TC7710WBG is communicated on I<sup>2</sup>C format. So, the packets divided by Start Condition / Stop Condition are transmitted and received. The communication consists of SCL (clock line) and SDA (data line). If they don't communicate, both clock line and data line are fixed to High level. It goes through Start Condition that data line goes down earlier than clock line. And it goes through Stop Condition that clock line goes down earlier than data line. It is prohibited changing condition of the data line, while the clock line is High level in normal communication.

It regards as the end of the communication, if the receiver doesn't operate that data line with low level in the timing which it receives ACK bit. And, after the end of the communication, it is possible to restart from Start Condition without Stop Condition.

**7.22.3 ACK data**

The receiver notifies the transceiver of ACK data by receiving 1 byte (8 bits) to indicate its condition. If it is no problems, it operates data line with low level after the clock of byte 8 (LSB) goes down. If the data communication error has occurred by any problems, the TC7710WBG reports NACK.

**7.22.4 Slave Address**

The TC7710WBG can choose the Slave Address that has 8 types by the fixed e-fuse data.

**Table 7-22 Slave Address**

	MSB							LSB
Address	0	0	0	1	0	0	1	R/ $\bar{W}$
	0	0	0	1	0	0	0	R/ $\bar{W}$
	0	0	0	1	0	1	1	R/ $\bar{W}$
	0	0	0	1	1	0	1	R/ $\bar{W}$
	0	0	1	1	0	0	1	R/ $\bar{W}$
	0	1	0	1	0	0	1	R/ $\bar{W}$
	1	0	0	1	0	0	1	R/ $\bar{W}$

**7.22.5 Write bytes**

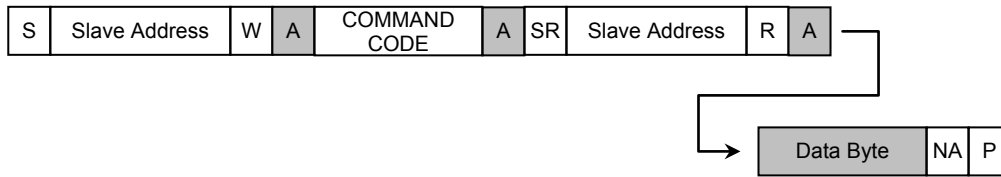
It transmits in order of an Slave Address, COMMAND CODE and Data Byte.



**Figure 7-3 Write bytes**

**7.22.6 Read bytes**

If the following bit of Slave Address is set to “1”, the TC7710WBG is selected in Read mode. The TC7710WBG sends the data that is issued by COMMAND CODE to the host, just before selected in Read mode.



**Figure 7-4 Read bytes**

**7.23 Cautions in writing I<sup>2</sup>C register**

To avoid a transitional response of operating parameter by I<sup>2</sup>C register rewriting, the TC7710WBG stops an internal operation change for about 250µs after I<sup>2</sup>C register writing. So if I<sup>2</sup>C register is written successively in 250µs, internal operation remains stopping in the meantime. And register is written normally. If programmed parameters are rewritten continuously after writing the charge EN control register and the OTG control register, charge and OTG operation do not start while I<sup>2</sup>C register is under writing. So rewrite parameter first, then rewrite of the EN control register and the OTG control register. As for reading of I<sup>2</sup>C register, internal operation does not stop.

**8. Register Map**

Address=00H

bit	Command	R/W	Initial value	Contents								
7	DBATVDET	R/W	1	Dead battery voltage threshold <table border="1"> <tr> <td>0</td> <td>VBATT &lt; 3.47V</td> </tr> <tr> <td>1</td> <td>VBATT &lt; 3.54V</td> </tr> </table>	0	VBATT < 3.47V	1	VBATT < 3.54V				
0	VBATT < 3.47V											
1	VBATT < 3.54V											
6	ATRCHGTH	R/W	0	Automatic re-charge voltage threshold <table border="1"> <tr> <td>0</td> <td>140mV</td> </tr> <tr> <td>1</td> <td>140mV</td> </tr> </table>	0	140mV	1	140mV				
0	140mV											
1	140mV											
5	CEI1	R/W	0	Charge completion current <table border="1"> <tr> <td>00</td> <td>50mA *Unavailable</td> </tr> <tr> <td>01</td> <td>100mA</td> </tr> <tr> <td>10</td> <td>150mA</td> </tr> <tr> <td>11</td> <td>200mA</td> </tr> </table> Initial state: "01"=100mA	00	50mA *Unavailable	01	100mA	10	150mA	11	200mA
00	50mA *Unavailable											
01	100mA											
10	150mA											
11	200mA											
4	CEI0	R/W	1									
3	-	R	0	-								
2	-	R	0	-								
1	PCI1	R/W	0	Pre-charge current <table border="1"> <tr> <td>00</td> <td>50mA</td> </tr> <tr> <td>01</td> <td>100mA</td> </tr> <tr> <td>10</td> <td>150mA</td> </tr> <tr> <td>11</td> <td>200mA</td> </tr> </table>	00	50mA	01	100mA	10	150mA	11	200mA
00	50mA											
01	100mA											
10	150mA											
11	200mA											
0	PCI0	R/W	1									

**Address=01H**

bit	Command	R/W	Initial value	Contents																																				
7	CCI4	R/W	0	Fast charge current <table border="1"> <tr><td>00000</td><td>300mA</td><td>01001</td><td>1,200mA</td></tr> <tr><td>00001</td><td>400mA</td><td>01010</td><td>1,300mA</td></tr> <tr><td>00010</td><td>500mA</td><td>01011</td><td>1,400mA</td></tr> <tr><td>00011</td><td>600mA</td><td>01100</td><td>1,500mA</td></tr> <tr><td>00100</td><td>700mA</td><td>01101</td><td>1,600mA</td></tr> <tr><td>00101</td><td>800mA</td><td>01110</td><td>1,700mA</td></tr> <tr><td>00110</td><td>900mA</td><td>01111</td><td>1,800mA</td></tr> <tr><td>00111</td><td>1,000mA</td><td>10000</td><td>1,900mA</td></tr> <tr><td>01000</td><td>1,100mA</td><td>10001</td><td>2,000mA</td></tr> </table>	00000	300mA	01001	1,200mA	00001	400mA	01010	1,300mA	00010	500mA	01011	1,400mA	00011	600mA	01100	1,500mA	00100	700mA	01101	1,600mA	00101	800mA	01110	1,700mA	00110	900mA	01111	1,800mA	00111	1,000mA	10000	1,900mA	01000	1,100mA	10001	2,000mA
00000	300mA	01001	1,200mA																																					
00001	400mA	01010	1,300mA																																					
00010	500mA	01011	1,400mA																																					
00011	600mA	01100	1,500mA																																					
00100	700mA	01101	1,600mA																																					
00101	800mA	01110	1,700mA																																					
00110	900mA	01111	1,800mA																																					
00111	1,000mA	10000	1,900mA																																					
01000	1,100mA	10001	2,000mA																																					
6	CCI3	R/W	0																																					
5	CCI2	R/W	0																																					
4	CCI1	R/W	1																																					
				00010	500mA	01011	1,400mA																																	
				00011	600mA	01100	1,500mA																																	
				00100	700mA	01101	1,600mA																																	
				00101	800mA	01110	1,700mA																																	
				00110	900mA	01111	1,800mA																																	
				00111	1,000mA	10000	1,900mA																																	
				01000	1,100mA	10001	2,000mA																																	
3	CCI0	R/W	0	Initial value: "00010"=500mA																																				
				OTG current limit *only OTG is enabled																																				
				00010	500mA	01100	1,500mA																																	
				00111	1000mA	01111	1,800mA																																	
				Initial value: "00010"=500mA																																				
2	CCVTH2	R/W	1	Threshold voltage from pre-charge to fast charge <table border="1"> <tr><td>000</td><td>2.6V</td><td>100</td><td>3.0V</td></tr> <tr><td>001</td><td>2.7V</td><td>101</td><td>3.1V</td></tr> <tr><td>010</td><td>2.8V</td><td>110</td><td>3.2V</td></tr> <tr><td>011</td><td>2.9V</td><td>111</td><td>3.3V</td></tr> </table>	000	2.6V	100	3.0V	001	2.7V	101	3.1V	010	2.8V	110	3.2V	011	2.9V	111	3.3V																				
000	2.6V	100	3.0V																																					
001	2.7V	101	3.1V																																					
010	2.8V	110	3.2V																																					
011	2.9V	111	3.3V																																					
1	CCVTH1	R/W	0																																					
0	CCVTH0	R/W	0																																					
				Initial value is 3.0V.																																				

**Address=02H**

bit	Command	R/W	Initial value	Contents														
7	-	R	0	-														
6	FLTV6	R/W	0	Float voltage <table border="1"> <tr><td>0000000</td><td>3.46V</td></tr> <tr><td>0000001</td><td>3.47V</td></tr> <tr><td>0000010</td><td>3.48V</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1111101</td><td>4.71V</td></tr> <tr><td>1111110</td><td>4.72V</td></tr> <tr><td>1111111</td><td>4.73V</td></tr> </table>	0000000	3.46V	0000001	3.47V	0000010	3.48V	:	:	1111101	4.71V	1111110	4.72V	1111111	4.73V
0000000	3.46V																	
0000001	3.47V																	
0000010	3.48V																	
:	:																	
1111101	4.71V																	
1111110	4.72V																	
1111111	4.73V																	
5	FLTV5	R/W	0															
4	FLTV4	R/W	0															
3	FLTV3	R/W	0															
2	FLTV2	R/W	1															
1	FLTV1	R/W	0															
0	FLTV0	R/W	0															
				Initial value: "0000100"=3.50V														

**Address=03H**

bit	Command	R/W	Initial value	Contents																																				
7	ACILMT4	R/W	0	AC input current limit <table border="1"> <tr><td>00000</td><td>300mA</td><td>01001</td><td>1,200mA</td></tr> <tr><td>00001</td><td>400mA</td><td>01010</td><td>1,300mA</td></tr> <tr><td>00010</td><td>500mA</td><td>01011</td><td>1,400mA</td></tr> <tr><td>00011</td><td>600mA</td><td>01100</td><td>1,500mA</td></tr> <tr><td>00100</td><td>700mA</td><td>01101</td><td>1,600mA</td></tr> <tr><td>00101</td><td>800mA</td><td>01110</td><td>1,700mA</td></tr> <tr><td>00110</td><td>900mA</td><td>01111</td><td>1,800mA</td></tr> <tr><td>00111</td><td>1,000mA</td><td>10000</td><td>1,900mA</td></tr> <tr><td>01000</td><td>1,100mA</td><td>10001</td><td>2,000mA</td></tr> </table> Current values in above table are maximum limit current. Initial value is 500mA.	00000	300mA	01001	1,200mA	00001	400mA	01010	1,300mA	00010	500mA	01011	1,400mA	00011	600mA	01100	1,500mA	00100	700mA	01101	1,600mA	00101	800mA	01110	1,700mA	00110	900mA	01111	1,800mA	00111	1,000mA	10000	1,900mA	01000	1,100mA	10001	2,000mA
00000	300mA	01001	1,200mA																																					
00001	400mA	01010	1,300mA																																					
00010	500mA	01011	1,400mA																																					
00011	600mA	01100	1,500mA																																					
00100	700mA	01101	1,600mA																																					
00101	800mA	01110	1,700mA																																					
00110	900mA	01111	1,800mA																																					
00111	1,000mA	10000	1,900mA																																					
01000	1,100mA	10001	2,000mA																																					
6	ACILMT3	R/W	0																																					
5	ACILMT2	R/W	0																																					
4	ACILMT1	R/W	1																																					
3	ACILMT0	R/W	0																																					
2	-	R	0	-																																				
1	ATLMTTH1	R/W	0	Automatic input current limit threshold <table border="1"> <tr><td>00</td><td>4.25V</td></tr> <tr><td>01</td><td>4.50V</td></tr> <tr><td>10</td><td>4.75V</td></tr> <tr><td>11</td><td>5.00V</td></tr> </table> Initial value: "01"=4.5V	00	4.25V	01	4.50V	10	4.75V	11	5.00V																												
00	4.25V																																							
01	4.50V																																							
10	4.75V																																							
11	5.00V																																							
0	ATLMTTH0	R/W	1																																					

**Address=04H**

bit	Command	R/W	Initial value	Contents								
7	-	R	0	-								
6	-	R	0	-								
5	OTGVCTL1	R/W	0	OTG output voltage <table border="1"> <tr><td>00</td><td>5.0V</td></tr> <tr><td>01</td><td>5.1V</td></tr> <tr><td>10</td><td>5.2V</td></tr> <tr><td>11</td><td>5.3V</td></tr> </table> Initial value: "00"=5.0V	00	5.0V	01	5.1V	10	5.2V	11	5.3V
00	5.0V											
01	5.1V											
10	5.2V											
11	5.3V											
4	OTGVCTL0	R/W	0									
3	-	R	0	-								
2	-	R	0	-								
1	OTGUVTH1	R/W	0	UVLO threshold in OTG mode <table border="1"> <tr><td>00</td><td>2.75V</td></tr> <tr><td>01</td><td>3.00V</td></tr> <tr><td>10</td><td>3.25V</td></tr> <tr><td>11</td><td>3.50V</td></tr> </table> Initial value: "00"=2.75V	00	2.75V	01	3.00V	10	3.25V	11	3.50V
00	2.75V											
01	3.00V											
10	3.25V											
11	3.50V											
0	OTGUVTH0	R/W	0									

**Address=05H**

bit	Command	R/W	Initial value	Contents								
7	-	R	0	-								
6	-	R	0	-								
5	-	R	0	-								
4	-	R	0	-								
3	-	R	0	-								
2	-	R	0	-								
1	OVTHL1	R/W	1	Over charge threshold voltage <table border="1" style="margin-left: 20px;"> <tr> <td>00</td> <td>200mV</td> </tr> <tr> <td>01</td> <td>150mV</td> </tr> <tr> <td>10</td> <td>100mV * Not recommended</td> </tr> <tr> <td>11</td> <td>50mV * Not recommended</td> </tr> </table>	00	200mV	01	150mV	10	100mV * Not recommended	11	50mV * Not recommended
00	200mV											
01	150mV											
10	100mV * Not recommended											
11	50mV * Not recommended											
0	OVTHL0	R/W	0	Initial value: "10"=100mV Notice: Please use 150mV or 200mV setting instead of initial value. Over charge threshold voltage: Float voltage + $\alpha$ (setting voltage of this register) corresponds to over-charge voltage threshold.								

**Address=10H**

bit	Command	R/W	Initial value	Contents				
7	-	R	0	-				
6	CHGTMCLR	R/W	0	<p>Pre-charge safety timer / Charge safety timer clear</p> <table border="1"> <tr> <td>0</td> <td>Timer operation</td> </tr> <tr> <td>1</td> <td>Both of charge timers are cleared. (Pulse command) In this time, status information of pre-charge and charge timer is cleared.</td> </tr> </table>	0	Timer operation	1	Both of charge timers are cleared. (Pulse command) In this time, status information of pre-charge and charge timer is cleared.
0	Timer operation							
1	Both of charge timers are cleared. (Pulse command) In this time, status information of pre-charge and charge timer is cleared.							
5	STBWDTM	R/W	0	<p>Standby WD timer</p> <table border="1"> <tr> <td>0</td> <td>42sec WDT: Invalid</td> </tr> <tr> <td>1</td> <td>42sec WDT: Valid</td> </tr> </table> <p>If the TC7710WBG is controlled by I<sup>2</sup>C before DCIN is inputted, standby WD timer should be valid.</p>	0	42sec WDT: Invalid	1	42sec WDT: Valid
0	42sec WDT: Invalid							
1	42sec WDT: Valid							
4	OTGWDTM	R/W	0	<p>OTG WD timer</p> <table border="1"> <tr> <td>0</td> <td>42sec WDT: Invalid</td> </tr> <tr> <td>1</td> <td>42sec WDT: Valid</td> </tr> </table> <p>OTG WD timer should be valid in OTG mode.</p>	0	42sec WDT: Invalid	1	42sec WDT: Valid
0	42sec WDT: Invalid							
1	42sec WDT: Valid							
3	CHGWDTM	R/W	0	<p>Charge WD timer</p> <table border="1"> <tr> <td>0</td> <td>42sec WDT: Invalid</td> </tr> <tr> <td>1</td> <td>42sec WDT: Valid</td> </tr> </table>	0	42sec WDT: Invalid	1	42sec WDT: Valid
0	42sec WDT: Invalid							
1	42sec WDT: Valid							
2	PRCHGTM	R/W	0	<p>Pre-charge safety timer</p> <table border="1"> <tr> <td>0</td> <td>36min timer: Valid</td> </tr> <tr> <td>1</td> <td>36min timer: Invalid</td> </tr> </table>	0	36min timer: Valid	1	36min timer: Invalid
0	36min timer: Valid							
1	36min timer: Invalid							
1	CHGSTM	R/W	0	<p>Charge safety timer</p> <table border="1"> <tr> <td>0</td> <td>240min timer: Valid</td> </tr> <tr> <td>1</td> <td>240min timer: Invalid</td> </tr> </table>	0	240min timer: Valid	1	240min timer: Invalid
0	240min timer: Valid							
1	240min timer: Invalid							
0	TCSTON	R/W	1	<p>Trickle charge safety timer</p> <table border="1"> <tr> <td>0</td> <td>Pre-charge timer and charge timer do not operate in trickle charging.</td> </tr> <tr> <td>1</td> <td>Pre-charge timer and charge timer operate in trickle charging.</td> </tr> </table>	0	Pre-charge timer and charge timer do not operate in trickle charging.	1	Pre-charge timer and charge timer operate in trickle charging.
0	Pre-charge timer and charge timer do not operate in trickle charging.							
1	Pre-charge timer and charge timer operate in trickle charging.							

**Address=11H**

bit	Command	R/W	Initial value	Contents				
7	-	R	0	-				
6	-	R	0	-				
5	-	R	0	-				
4	BATMSDET	R/W	1	Unconnected battery detection <table border="1"> <tr> <td>0</td> <td>Invalid</td> </tr> <tr> <td>1</td> <td>Valid</td> </tr> </table>	0	Invalid	1	Valid
0	Invalid							
1	Valid							
3	ATCHG	R/W	1	Automatic charge control <table border="1"> <tr> <td>0</td> <td>Invalid (OFF in charge disable)</td> </tr> <tr> <td>1</td> <td>Valid (In charge disable, it is charged only when the battery voltage is lower than threshold.)</td> </tr> </table> (In charge enable, it is charged regardless of the battery voltage.) It is charged automatically when the battery voltage is lower than dead battery threshold.	0	Invalid (OFF in charge disable)	1	Valid (In charge disable, it is charged only when the battery voltage is lower than threshold.)
0	Invalid (OFF in charge disable)							
1	Valid (In charge disable, it is charged only when the battery voltage is lower than threshold.)							
2	ENSEL	R/W	0	EN is controlled by I <sup>2</sup> C or EN pin. <table border="1"> <tr> <td>0</td> <td>Controlled by EN pin. (Polarity is selected by ENPINPOL)</td> </tr> <tr> <td>1</td> <td>Controlled by I<sup>2</sup>C. (Selected by ENCMD.)</td> </tr> </table>	0	Controlled by EN pin. (Polarity is selected by ENPINPOL)	1	Controlled by I <sup>2</sup> C. (Selected by ENCMD.)
0	Controlled by EN pin. (Polarity is selected by ENPINPOL)							
1	Controlled by I <sup>2</sup> C. (Selected by ENCMD.)							
1	ENCMD	R/W	1	EN is controlled by I <sup>2</sup> C. <table border="1"> <tr> <td>0</td> <td>Enable (charger is tuned on.)</td> </tr> <tr> <td>1</td> <td>Disable (charger is turned off.)</td> </tr> </table>	0	Enable (charger is tuned on.)	1	Disable (charger is turned off.)
0	Enable (charger is tuned on.)							
1	Disable (charger is turned off.)							
0	ENPINPOL	R/W	0	Polarity of EN control is selected by EN pin. <table border="1"> <tr> <td>0</td> <td>"L" is active. ("L"=Enable, "H"=Disable)</td> </tr> <tr> <td>1</td> <td>"H" is active. ("L"=Disable, "H"=Enable)</td> </tr> </table>	0	"L" is active. ("L"=Enable, "H"=Disable)	1	"H" is active. ("L"=Disable, "H"=Enable)
0	"L" is active. ("L"=Enable, "H"=Disable)							
1	"H" is active. ("L"=Disable, "H"=Enable)							



**Address=12H**

bit	Command	R/W	Initial value	Contents				
7	TEMPDET	R/W	0	Battery thermal detection <table border="1"> <tr> <td>0</td> <td>Valid (Charging stops when the temperature exceeds the limit value. And charging re-starts automatically when the temperature falls within the range.)</td> </tr> <tr> <td>1</td> <td>Invalid (Charging does not stop though the temperature exceeds limit value.)</td> </tr> </table>	0	Valid (Charging stops when the temperature exceeds the limit value. And charging re-starts automatically when the temperature falls within the range.)	1	Invalid (Charging does not stop though the temperature exceeds limit value.)
0	Valid (Charging stops when the temperature exceeds the limit value. And charging re-starts automatically when the temperature falls within the range.)							
1	Invalid (Charging does not stop though the temperature exceeds limit value.)							
6	OVTLMT	R/W	1	IC temperature limit <table border="1"> <tr> <td>0</td> <td>Only status bit: Valid</td> </tr> <tr> <td>1</td> <td>Status bit: Valid. Permission of suspending charge.</td> </tr> </table>	0	Only status bit: Valid	1	Status bit: Valid. Permission of suspending charge.
0	Only status bit: Valid							
1	Status bit: Valid. Permission of suspending charge.							
5	BATOV	R/W	1	Battery OV <table border="1"> <tr> <td>0</td> <td>Charging cycle does not terminate when battery voltage is OV.</td> </tr> <tr> <td>1</td> <td>Charging cycle terminates when battery voltage is OV.</td> </tr> </table>	0	Charging cycle does not terminate when battery voltage is OV.	1	Charging cycle terminates when battery voltage is OV.
0	Charging cycle does not terminate when battery voltage is OV.							
1	Charging cycle terminates when battery voltage is OV.							
4	ATRCHG	R/W	0	Auto re-charge <table border="1"> <tr> <td>0</td> <td>Valid</td> </tr> <tr> <td>1</td> <td>Invalid</td> </tr> </table>	0	Valid	1	Invalid
0	Valid							
1	Invalid							
3	CT	R/W	0	Terminating <table border="1"> <tr> <td>0</td> <td>Permitting termination of charging cycle.</td> </tr> <tr> <td>1</td> <td>Not permitting termination of charging cycle.</td> </tr> </table> Charging is completed when charge current is lower than the value set by CEI1-0.	0	Permitting termination of charging cycle.	1	Not permitting termination of charging cycle.
0	Permitting termination of charging cycle.							
1	Not permitting termination of charging cycle.							
2	CCISSET	R/W	1	Fast charge setting (PRCCTH = "1": Valid) <table border="1"> <tr> <td>0</td> <td>Setting forced pre-charge current</td> </tr> <tr> <td>1</td> <td>Permission of setting fast charge current</td> </tr> </table>	0	Setting forced pre-charge current	1	Permission of setting fast charge current
0	Setting forced pre-charge current							
1	Permission of setting fast charge current							
1	PRCCTH	R/W	0	Threshold voltage from pre-charge to fast charge <table border="1"> <tr> <td>0</td> <td>Valid</td> </tr> <tr> <td>1</td> <td>Invalid</td> </tr> </table>	0	Valid	1	Invalid
0	Valid							
1	Invalid							
0	TRCHG	R/W	0	Trickle charge <table border="1"> <tr> <td>0</td> <td>Valid</td> </tr> <tr> <td>1</td> <td>Invalid</td> </tr> </table>	0	Valid	1	Invalid
0	Valid							
1	Invalid							

**Address=13H**

bit	Command	R/W	Initial value	Contents				
7	OTGMD	R/W	0	OTG mode <table border="1"> <tr> <td>0</td> <td>Invalid</td> </tr> <tr> <td>1</td> <td>Valid</td> </tr> </table>	0	Invalid	1	Valid
0	Invalid							
1	Valid							
6	USB51	R/W	0	Input current limit level set by ILIM_OTG pin in USB ("L" level). <table border="1"> <tr> <td>0</td> <td>USB500 mode</td> </tr> <tr> <td>1</td> <td>USB100 mode</td> </tr> </table> This setting is valid under the following condition. LMT_OTG1-0 = "01", ILIM_OTG pin="L".	0	USB500 mode	1	USB100 mode
0	USB500 mode							
1	USB100 mode							
5	ATILMT	R/W	0	Automatic input current limit <table border="1"> <tr> <td>0</td> <td>Valid</td> </tr> <tr> <td>1</td> <td>Invalid</td> </tr> </table> Input current limit is set USB100 when DCIN falls to the level set by ATLMTTH1-0. When an interrupt is cleared, it is set to previous limit level.	0	Valid	1	Invalid
0	Valid							
1	Invalid							
4	ATPSDET	R/W	0	Automatic power source detection <table border="1"> <tr> <td>0</td> <td>Valid</td> </tr> <tr> <td>1</td> <td>Invalid (Set level = Limit level)</td> </tr> </table>	0	Valid	1	Invalid (Set level = Limit level)
0	Valid							
1	Invalid (Set level = Limit level)							
3	LMT_OTG1	R/W	0	Input current limit and OTG control are set by pin or I <sup>2</sup> C. <table border="1"> <tr> <td>00</td> <td>Input current limit is set by I<sup>2</sup>C (ILIMLVL1-0). OTG mode is set by I<sup>2</sup>C (OTGMD).</td> </tr> <tr> <td>01</td> <td>Input current limit is set by ILIM_OTG pin.                              "L"= USB mode, USB51="L" -&gt; USB500 mode                              "L"= USB mode, USB51="H" -&gt; USB100 mode                              "H"=AC mode (set by ACILMT4-0)                              OTG mode is set by I<sup>2</sup>C (OTGMD).</td> </tr> </table>	00	Input current limit is set by I <sup>2</sup> C (ILIMLVL1-0). OTG mode is set by I <sup>2</sup> C (OTGMD).	01	Input current limit is set by ILIM_OTG pin. "L"= USB mode, USB51="L" -> USB500 mode "L"= USB mode, USB51="H" -> USB100 mode "H"=AC mode (set by ACILMT4-0) OTG mode is set by I <sup>2</sup> C (OTGMD).
00	Input current limit is set by I <sup>2</sup> C (ILIMLVL1-0). OTG mode is set by I <sup>2</sup> C (OTGMD).							
01	Input current limit is set by ILIM_OTG pin. "L"= USB mode, USB51="L" -> USB500 mode "L"= USB mode, USB51="H" -> USB100 mode "H"=AC mode (set by ACILMT4-0) OTG mode is set by I <sup>2</sup> C (OTGMD).							
2	LMT_OTG0	R/W	1	<table border="1"> <tr> <td>10</td> <td>Input current limit is set by I<sup>2</sup>C (ILIMLVL1-0). OTG mode is set by ILIM_OTG pin ("H" active).                              "L": Invalid, "H": Valid</td> </tr> <tr> <td>11</td> <td>Input current limit is set by I<sup>2</sup>C (ILIMLVL1-0). OTG mode is set by ILIM_OTG pin ("L" active).                              "L": Valid, "H": Invalid</td> </tr> </table>	10	Input current limit is set by I <sup>2</sup> C (ILIMLVL1-0). OTG mode is set by ILIM_OTG pin ("H" active). "L": Invalid, "H": Valid	11	Input current limit is set by I <sup>2</sup> C (ILIMLVL1-0). OTG mode is set by ILIM_OTG pin ("L" active). "L": Valid, "H": Invalid
10	Input current limit is set by I <sup>2</sup> C (ILIMLVL1-0). OTG mode is set by ILIM_OTG pin ("H" active). "L": Invalid, "H": Valid							
11	Input current limit is set by I <sup>2</sup> C (ILIMLVL1-0). OTG mode is set by ILIM_OTG pin ("L" active). "L": Valid, "H": Invalid							
1	ILIMLVL1	R/W	1	Input current limit level in I <sup>2</sup> C control. <table border="1"> <tr> <td>00</td> <td>USB500 mode (Typ. = 475mA, Max = 500mA)</td> </tr> <tr> <td>01</td> <td>USB100 mode (Typ. = 90mA, Max = 100mA)</td> </tr> </table>	00	USB500 mode (Typ. = 475mA, Max = 500mA)	01	USB100 mode (Typ. = 90mA, Max = 100mA)
00	USB500 mode (Typ. = 475mA, Max = 500mA)							
01	USB100 mode (Typ. = 90mA, Max = 100mA)							
0	ILIMLVL0	R/W	0	<table border="1"> <tr> <td>10</td> <td>AC mode (Set by ACILMT4-0.)</td> </tr> <tr> <td>11</td> <td>AC mode (Set by ACILMT4-0.)</td> </tr> </table> Initial value: "10" = AC mode.	10	AC mode (Set by ACILMT4-0.)	11	AC mode (Set by ACILMT4-0.)
10	AC mode (Set by ACILMT4-0.)							
11	AC mode (Set by ACILMT4-0.)							

**Address=14H**

bit	Command	R/W	Initial value	Contents				
7	-	R	0	-				
6	-	R	0	-				
5	-	R	0	-				
4	VMONICNT	R/W	0	VMONI control <table border="1"> <tr> <td>0</td> <td>Valid</td> </tr> <tr> <td>1</td> <td>Invalid</td> </tr> </table>	0	Valid	1	Invalid
0	Valid							
1	Invalid							
3	INTOUT	R/W	0	Information from STAT pin is selected. <table border="1"> <tr> <td>0</td> <td>Status information is outputted. (Information is set by STATMD. STATOUT = "0": Output is valid.)</td> </tr> <tr> <td>1</td> <td>Interrupt output (STATOUT = "1": Interrupt information is valid.)</td> </tr> </table>	0	Status information is outputted. (Information is set by STATMD. STATOUT = "0": Output is valid.)	1	Interrupt output (STATOUT = "1": Interrupt information is valid.)
0	Status information is outputted. (Information is set by STATMD. STATOUT = "0": Output is valid.)							
1	Interrupt output (STATOUT = "1": Interrupt information is valid.)							
2	STATMD	R/W	0	Information from STAT pin is selected. <table border="1"> <tr> <td>0</td> <td>Charging state is indicated.</td> </tr> <tr> <td>1</td> <td>State of input UV/OV is indicated.</td> </tr> </table>	0	Charging state is indicated.	1	State of input UV/OV is indicated.
0	Charging state is indicated.							
1	State of input UV/OV is indicated.							
1	STATOUT	R/W	0	Output of STAT pin: ON/OFF <table border="1"> <tr> <td>0</td> <td>ON</td> </tr> <tr> <td>1</td> <td>OFF</td> </tr> </table>	0	ON	1	OFF
0	ON							
1	OFF							
0	SFTRST	R/W	0	Soft reset command <table border="1"> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>Internal reset (Pulse command)</td> </tr> </table> Register is cleared and default value is reloaded.	0	OFF	1	Internal reset (Pulse command)
0	OFF							
1	Internal reset (Pulse command)							

**Address=15H**

bit	Command	R/W	Initial value	Contents
7	INTCLR7	R	0	Interrupt factor is cleared. Interrupt factor for each bit of 20h is cleared. (Pulse command)
6	INTCLR6	R/W	0	
5	INTCLR5	R/W	0	
4	INTCLR4	R/W	0	
3	INTCLR3	R/W	0	
2	INTCLR2	R/W	0	
1	INTCLR1	R/W	0	
0	INTCLR0	R/W	0	

**Address=16H**

bit	Command	R/W	Initial value	Contents				
7	INTMSK7	R	0	Interrupt output from STAT pin is masked. (Interrupt information is active regardless of state of this bit.) <table border="1" style="margin-left: 20px;"> <tr> <td>0</td> <td>Interrupt factor is not masked.</td> </tr> <tr> <td>1</td> <td>Interrupt factor is masked.</td> </tr> </table>	0	Interrupt factor is not masked.	1	Interrupt factor is masked.
0	Interrupt factor is not masked.							
1	Interrupt factor is masked.							
6	INTMSK6	R/W	1					
5	INTMSK5	R/W	1					
4	INTMSK4	R/W	1					
3	INTMSK3	R/W	1					
2	INTMSK2	R/W	1					
1	INTMSK1	R/W	1					
0	INTMSK0	R/W	1					

**Address=1EH**

bit	Command	R/W	Initial value	Contents								
7	BIASCRT1	R/W	0	Current source for temperature monitoring <table border="1" style="margin-left: 20px;"> <tr> <td>00</td> <td>200<math>\mu</math>A</td> </tr> <tr> <td>01</td> <td>80<math>\mu</math>A</td> </tr> <tr> <td>10</td> <td>40<math>\mu</math>A</td> </tr> <tr> <td>11</td> <td>20<math>\mu</math>A</td> </tr> </table>	00	200 $\mu$ A	01	80 $\mu$ A	10	40 $\mu$ A	11	20 $\mu$ A
00	200 $\mu$ A											
01	80 $\mu$ A											
10	40 $\mu$ A											
11	20 $\mu$ A											
6	BIASCRT0	R/W	0									
5	-	R	0	-								
4	-	R	0	-								
3	COLDVTH1	R/W	0	Threshold level for low temperature judge <table border="1" style="margin-left: 20px;"> <tr> <td>00</td> <td>1.399V</td> </tr> <tr> <td>01</td> <td>1.491V</td> </tr> <tr> <td>10</td> <td>1.577V</td> </tr> <tr> <td>11</td> <td>1.654V</td> </tr> </table>	00	1.399V	01	1.491V	10	1.577V	11	1.654V
00	1.399V											
01	1.491V											
10	1.577V											
11	1.654V											
2	COLDVTH0	R/W	0									
1	HOTVTH1	R/W	0	Threshold level for high temperature judge <table border="1" style="margin-left: 20px;"> <tr> <td>00</td> <td>0.509V</td> </tr> <tr> <td>01</td> <td>0.574V</td> </tr> <tr> <td>10</td> <td>0.647V</td> </tr> <tr> <td>11</td> <td>0.726V</td> </tr> </table>	00	0.509V	01	0.574V	10	0.647V	11	0.726V
00	0.509V											
01	0.574V											
10	0.647V											
11	0.726V											
0	HOTVTH0	R/W	1									

**Address=1FH**

bit	Command	R/W	Initial value	Contents																
7	-	R	0	-																
6	-	R	0	-																
5	-	R	0	-																
4	-	R	0	-																
3	-	R	0	-																
2	I2CSVAD2	R/W	0	I <sup>2</sup> C slave address <table border="1"> <tr> <td>000</td> <td>No conversion -&gt; 0001001</td> </tr> <tr> <td>001</td> <td>Convert bit0 -&gt; 0001000</td> </tr> <tr> <td>010</td> <td>Convert bit1 -&gt; 0001011</td> </tr> <tr> <td>011</td> <td>Convert bit2 -&gt; 0001101</td> </tr> <tr> <td>100</td> <td>Convert bit3 -&gt; 0000001 *Reserved: CBUS address</td> </tr> <tr> <td>101</td> <td>Convert bit4 -&gt; 0011001</td> </tr> <tr> <td>110</td> <td>Convert bit5 -&gt; 0101001</td> </tr> <tr> <td>111</td> <td>Convert bit6 -&gt; 1001001</td> </tr> </table>	000	No conversion -> 0001001	001	Convert bit0 -> 0001000	010	Convert bit1 -> 0001011	011	Convert bit2 -> 0001101	100	Convert bit3 -> 0000001 *Reserved: CBUS address	101	Convert bit4 -> 0011001	110	Convert bit5 -> 0101001	111	Convert bit6 -> 1001001
000	No conversion -> 0001001																			
001	Convert bit0 -> 0001000																			
010	Convert bit1 -> 0001011																			
011	Convert bit2 -> 0001101																			
100	Convert bit3 -> 0000001 *Reserved: CBUS address																			
101	Convert bit4 -> 0011001																			
110	Convert bit5 -> 0101001																			
111	Convert bit6 -> 1001001																			
1	I2CSVAD1	R/W	0																	
0	I2CSVAD0	R/W	0																	

**Address=20H**

bit	Command	R/W	Initial value	Contents
7	-	R	0	-
6	INTVBAT	R	0	1: Charge state is back to previous mode by battery voltage drop.
5	INTATIL	R	0	1: Automatic input current limit is occurred.
4	INTSTBER	R	0	Interrupt of standby WDT error 1: WDT error is occurred. Register of 00H - 13H, 1EH and 1FH are initialized.
3	INTOTGER	R	0	Interrupt of OTG error (Interrupt factor should be confirmed 22H) 1: OTG error is occurred.
2	INTRCHG	R	0	Interrupt of re-charge 1: Re-charge
1	INTCHGER	R	0	Interrupt of charge error (Interrupt factor should be confirmed 21H and 23H.) 1: Charge error is occurred.
0	INTTERMN	R	0	Interrupt of charge complete. However, it is valid only when CT (12H, bit3) is "0". 1: Charge completion

**Address=21H**

bit	Command	R/W	Initial value	Contents
7	ST_BATMS	R	0	Status 1: Unconnected battery detected.
6	ST_VBATN	R	-	Status: Initial value depends on DCIN voltage and battery voltage. 1: DCIN < VBATT
5	ST_BATOV	R	-	Status: Initial value depends on battery voltage. 1: Battery OVLO
4	ST_DCOVL	R	-	Status: Initial value depends on DCIN input voltage. 1: Input OVLO
3	ST_DCUVL	R	-	Status: Initial value depends on DCIN input voltage. 1: Input UVLO
2	ST_JCTON	R	-	Status: Initial value depends on chip temperature. It operates though in charging or OTG mode. Chip temperature $\geq 135^{\circ}\text{C}$ : 1, Chip temperature $\leq 115^{\circ}\text{C}$ : 0 1: Internal temperature is limited.
1	ST_BATHT	R	-	Status: Initial value depends on battery temperature. 1: High temperature detected
0	ST_BATCL	R	-	Status: Initial value depends on battery temperature. 1: Low temperature detected

**Address=22H**

bit	Command	R/W	Initial value	Contents
7	-	R	0	-
6	-	R	0	-
5	-	R	0	-
4	ST_OTGVOL	R	0	Status: It shows "0" for 250ms after starting OTG. 1: Output voltage drops under DCIN UVLO.
3	ST_OTGJCT	R	-	Status: Initial value depends on chip temperature. It operates though in charging or OTG mode. Chip temperature $\geq 135^{\circ}\text{C}$ : 1, Chip temperature $\leq 115^{\circ}\text{C}$ : 0. 1: Internal temperature limited.
2	ST_OTWDT	R	0	Status 1: WDT error occurred. OTG supply is shut off. Registers of 00H-13H, 1EH and 1FH are initialized.
1	ST_OTGLM	R	-	Status: Initial value depends on OTG current. 1: OTG current limit reached
0	ST_OTUVL	R	-	Status: Initial value depends on battery voltage. 1: OTG battery UVLO

**Address=23H**

bit	Command	R/W	Initial value	Contents								
7	-	R	0	-								
6	-	R	0	-								
5	-	R	0	-								
4	-	R	0	-								
3	-	R	0	-								
2	ST_CHWDT	R	0	Status 1: WDT error occurred. Charging stops. Register of 00H-13H, 1EH and 1FH are initialized. However, only charging timer operates continuously.								
1	ST_TMER1	R	1	Status: Safety timer <table border="1"> <tr> <td>00</td> <td>No timeout occurred.</td> </tr> <tr> <td>01</td> <td>Pre-charge timer expired.</td> </tr> <tr> <td>10</td> <td>Charge timer expired.</td> </tr> <tr> <td>11</td> <td>Waiting to start charge</td> </tr> </table>	00	No timeout occurred.	01	Pre-charge timer expired.	10	Charge timer expired.	11	Waiting to start charge
00	No timeout occurred.											
01	Pre-charge timer expired.											
10	Charge timer expired.											
11	Waiting to start charge											
0	ST_TMER0	R	1									

**Address=24H**

bit	Command	R/W	Initial value	Contents								
7	ST_OTGMD	R	0	Status 1: OTG in progress								
6	-	R	0	-								
5	ST_CGED1	R	0	Status: Charge completion 1: At least, one charge cycle starts and completes.								
4	ST_CGED0	R	-	Status: Charge completion Initial value depends on charge current. 1: Charge current is lower than charge completion current (Valid only in CV charge mode.).								
3	ST_TRCHG	R	0	Status 1: Trickle charge mode (VBATT < 2.1V)								
2	ST_CGMD1	R	0	Status: Charging <table border="1"> <tr> <td>00</td> <td>No charge</td> </tr> <tr> <td>01</td> <td>Pre-charge</td> </tr> <tr> <td>10</td> <td>Constant current charge (CC mode)</td> </tr> <tr> <td>11</td> <td>Constant voltage charge (CV mode)</td> </tr> </table>	00	No charge	01	Pre-charge	10	Constant current charge (CC mode)	11	Constant voltage charge (CV mode)
00	No charge											
01	Pre-charge											
10	Constant current charge (CC mode)											
11	Constant voltage charge (CV mode)											
1	ST_CGMD0	R	0									
0	ST_CHGEN	R	0	Status: Charge valid / invalid <table border="1"> <tr> <td>0</td> <td>Charge invalid</td> </tr> <tr> <td>1</td> <td>Charge valid</td> </tr> </table>	0	Charge invalid	1	Charge valid				
0	Charge invalid											
1	Charge valid											

**Address=25H**

bit	Command	R/W	Initial value	Contents								
7	-	R	0	-								
6	-	R	0	-								
5	ST_USB51	R	*	Status: USB5/1 mode Initial value is determined by 13h, 6. <table border="1"> <tr> <td>0</td> <td>USB 100mA mode</td> </tr> <tr> <td>1</td> <td>USB 500mA mode</td> </tr> </table>	0	USB 100mA mode	1	USB 500mA mode				
0	USB 100mA mode											
1	USB 500mA mode											
4	ST_USBAC	R	0	Status: USB / AC mode <table border="1"> <tr> <td>0</td> <td>USB mode</td> </tr> <tr> <td>1</td> <td>AC mode</td> </tr> </table>	0	USB mode	1	AC mode				
0	USB mode											
1	AC mode											
3	ST_DTBSY	R	0	Status: Power source detection function <table border="1"> <tr> <td>0</td> <td>Not busy</td> </tr> <tr> <td>1</td> <td>Busy</td> </tr> </table>	0	Not busy	1	Busy				
0	Not busy											
1	Busy											
2	ST_PSDST	R	1	Status: Power source detection <table border="1"> <tr> <td>0</td> <td>Detecting</td> </tr> <tr> <td>1</td> <td>Finished (after source detected)</td> </tr> </table>	0	Detecting	1	Finished (after source detected)				
0	Detecting											
1	Finished (after source detected)											
1	ST_STYP1	R	0	Status: Power source type <table border="1"> <tr> <td>00</td> <td>Non connection</td> </tr> <tr> <td>01</td> <td>SDP (Standard Downstream Port)</td> </tr> <tr> <td>10</td> <td>CDP (Charging Downstream Port)</td> </tr> <tr> <td>11</td> <td>DCP (Dedicated Charging Port)</td> </tr> </table>	00	Non connection	01	SDP (Standard Downstream Port)	10	CDP (Charging Downstream Port)	11	DCP (Dedicated Charging Port)
00	Non connection											
01	SDP (Standard Downstream Port)											
10	CDP (Charging Downstream Port)											
11	DCP (Dedicated Charging Port)											
0	ST_STYP0	R	0									

**Address=26H**

bit	Command	R/W	Initial value	Contents		
7	-	R	0	-		
6	REVCODE2	R	0	Device revision code <table border="1"> <tr> <td>000</td> <td>#1.0</td> </tr> </table>	000	#1.0
000	#1.0					
5	REVCODE1	R	0			
4	REVCODE0	R	0			
3	-	R	0	-		
2	-	R	0	-		
1	-	R	0	-		
0	-	R	0	-		



9. Mode Transition Diagram

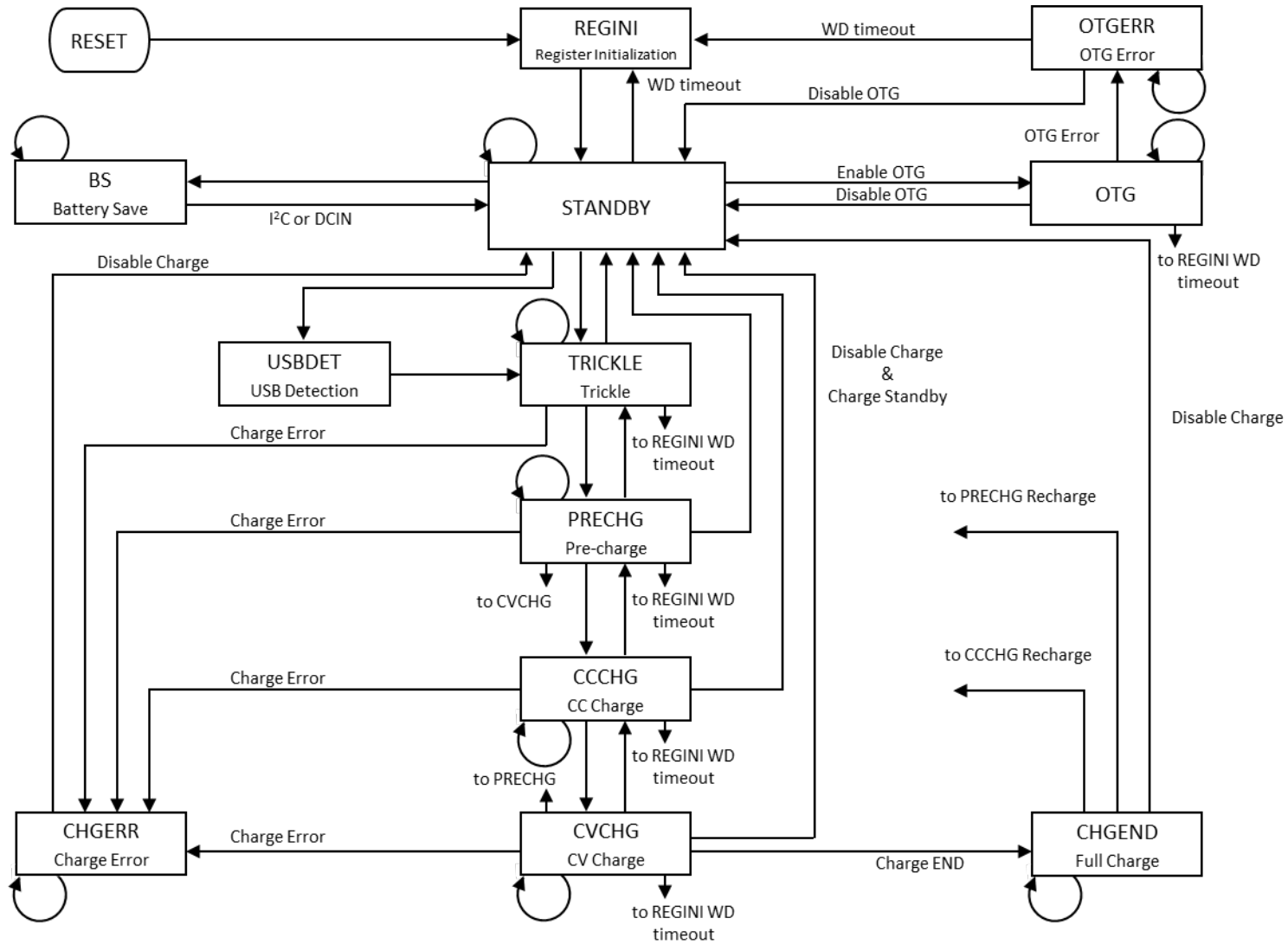


Figure 9-1 Mode transition diagram

10. Flow chart of function

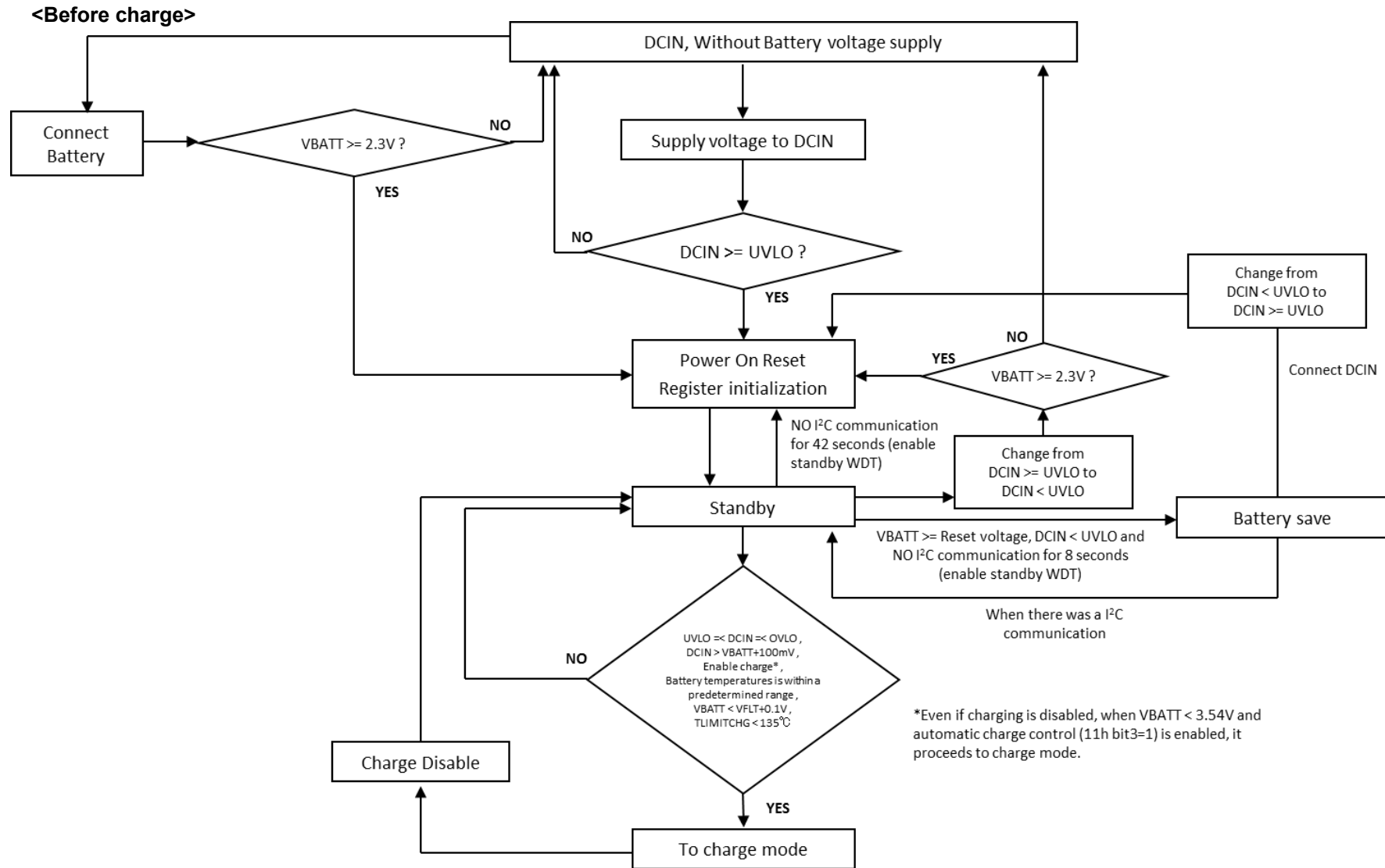


Figure 10-1 Flow chart: Before charge

<After start charging>

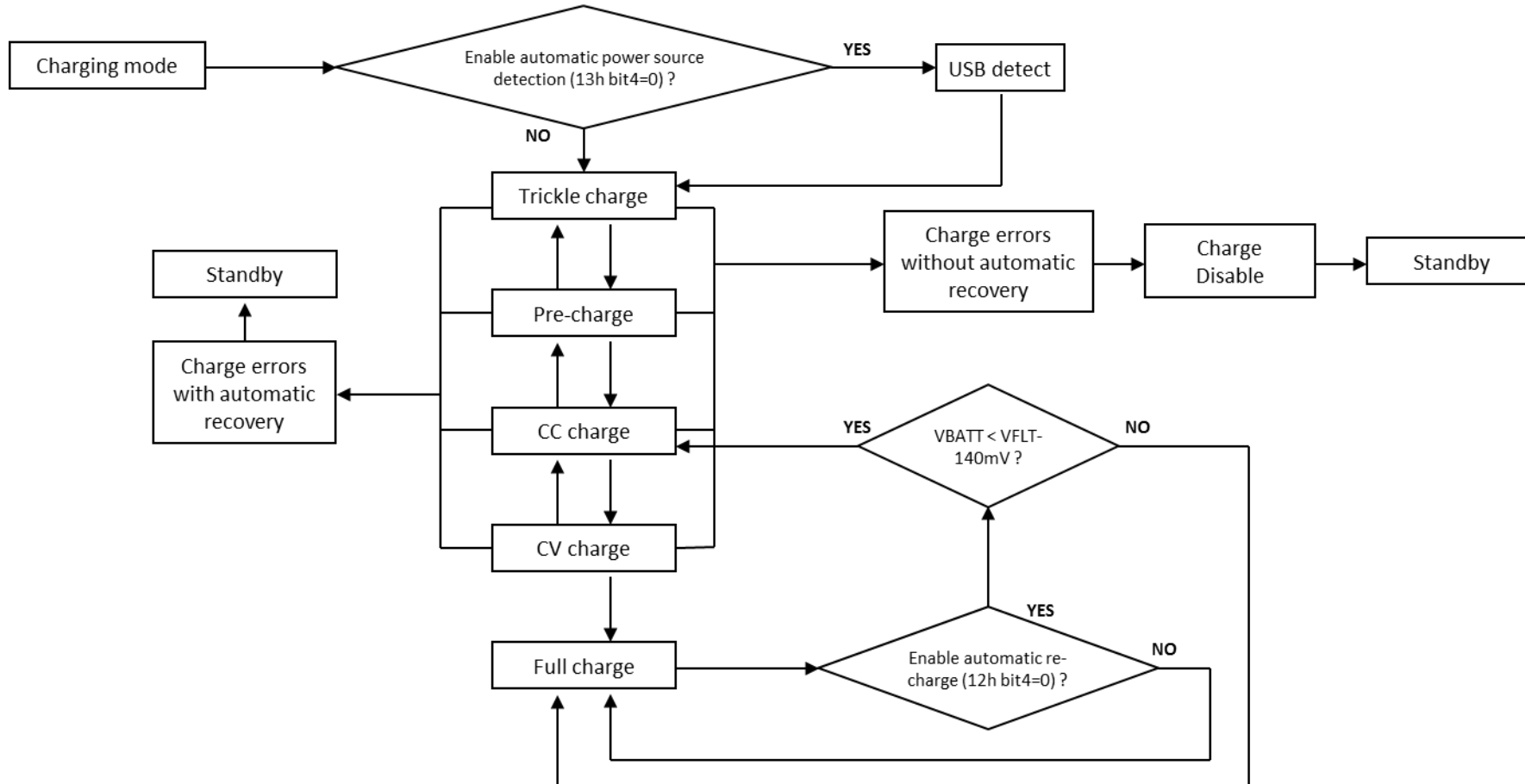


Figure 10-2 Flow chart: After start charging

<Trickle charge>

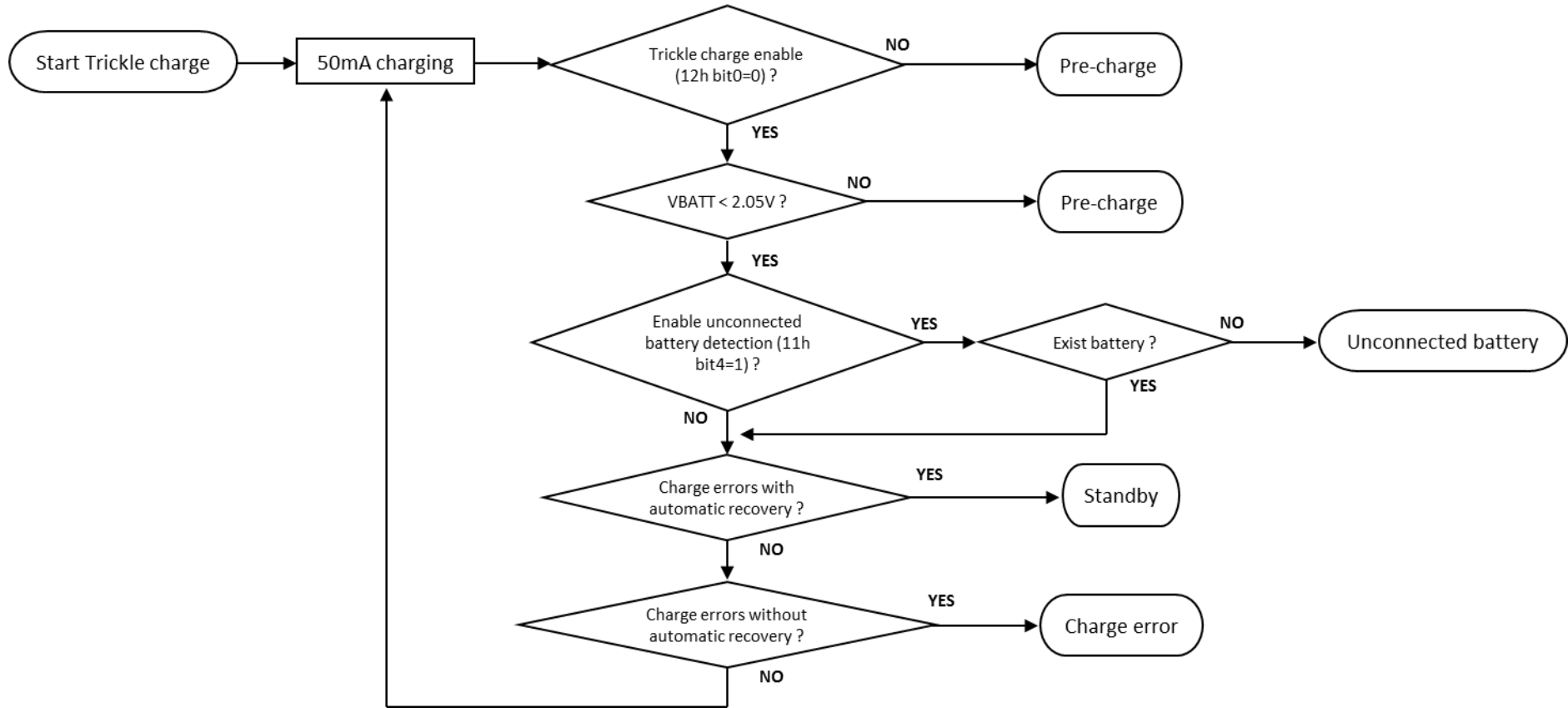


Figure 10-3 Flow chart: Trickle charge

<Pre charge>

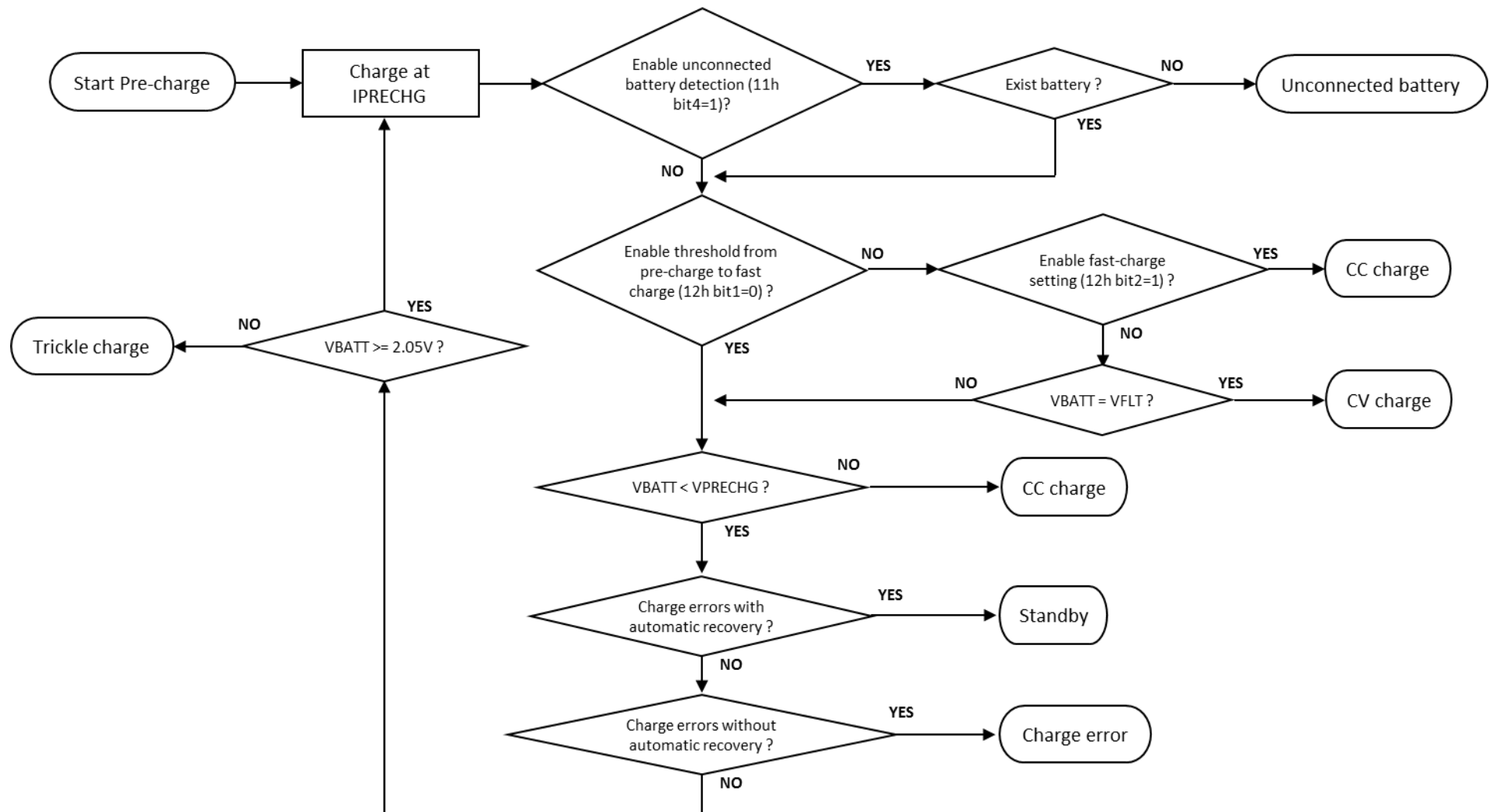


Figure 10-4 Flow chart: Pre-charge

<CC charge>

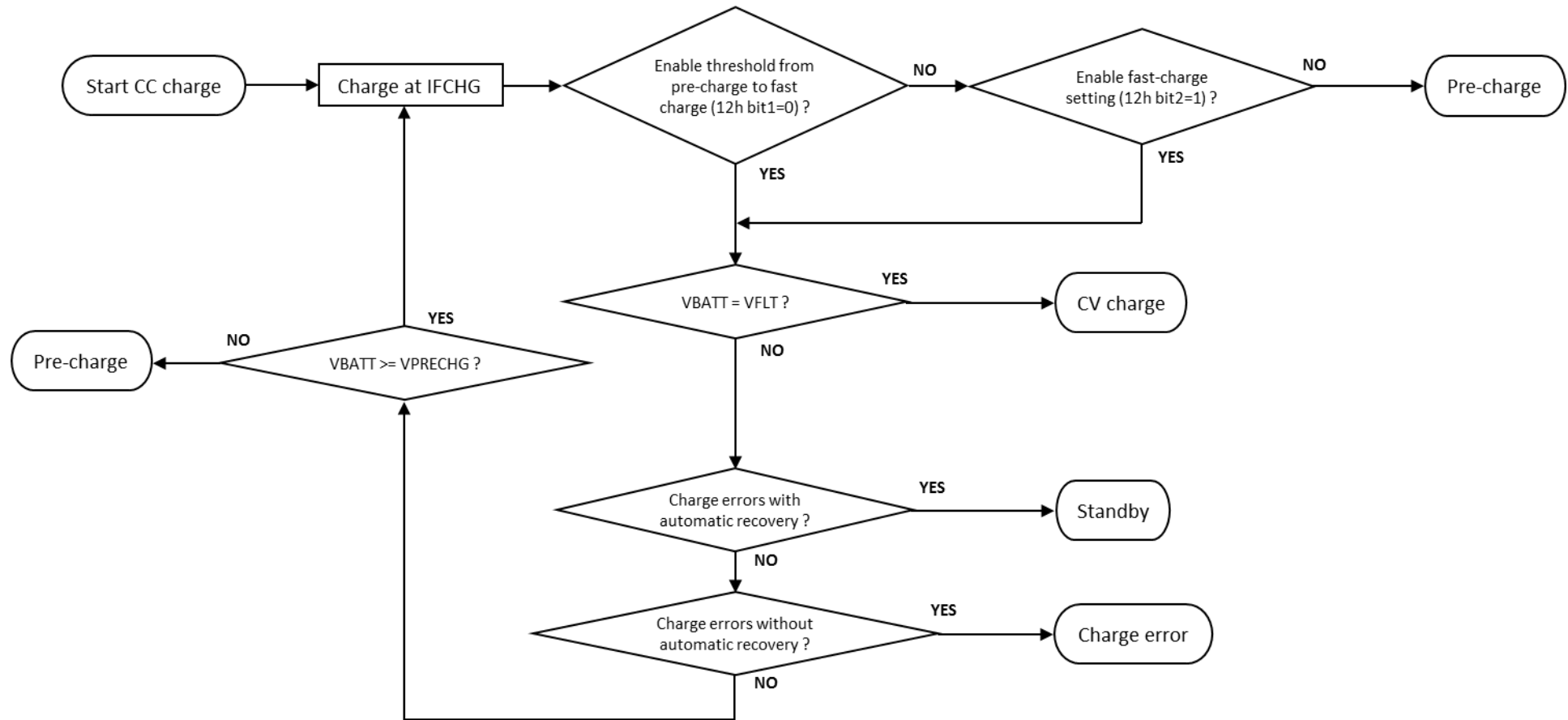


Figure 10-5 Flow chart: CC charge

<CV charge>

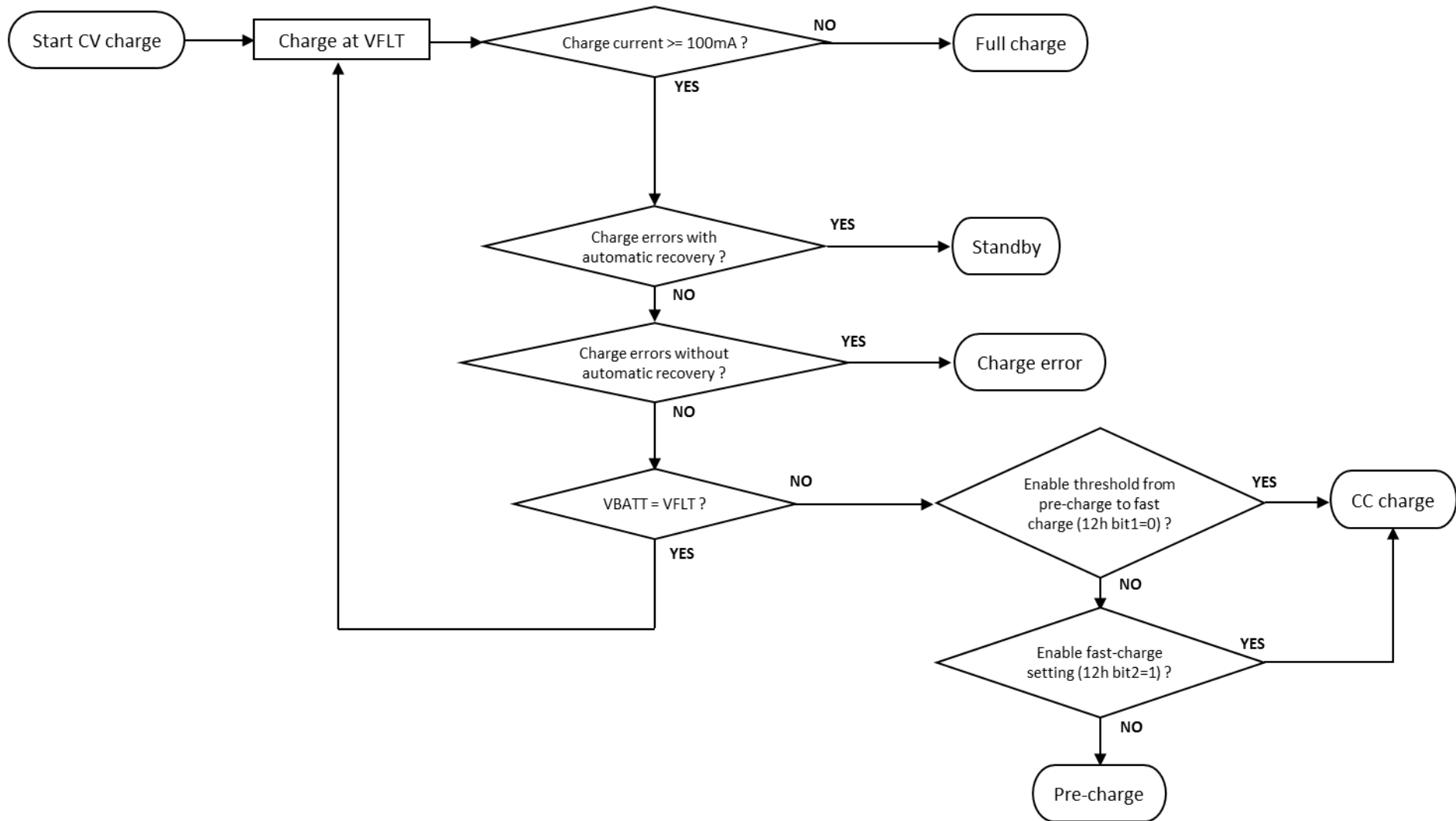


Figure 10-6 Flow chart: CV charge

<Full charge>

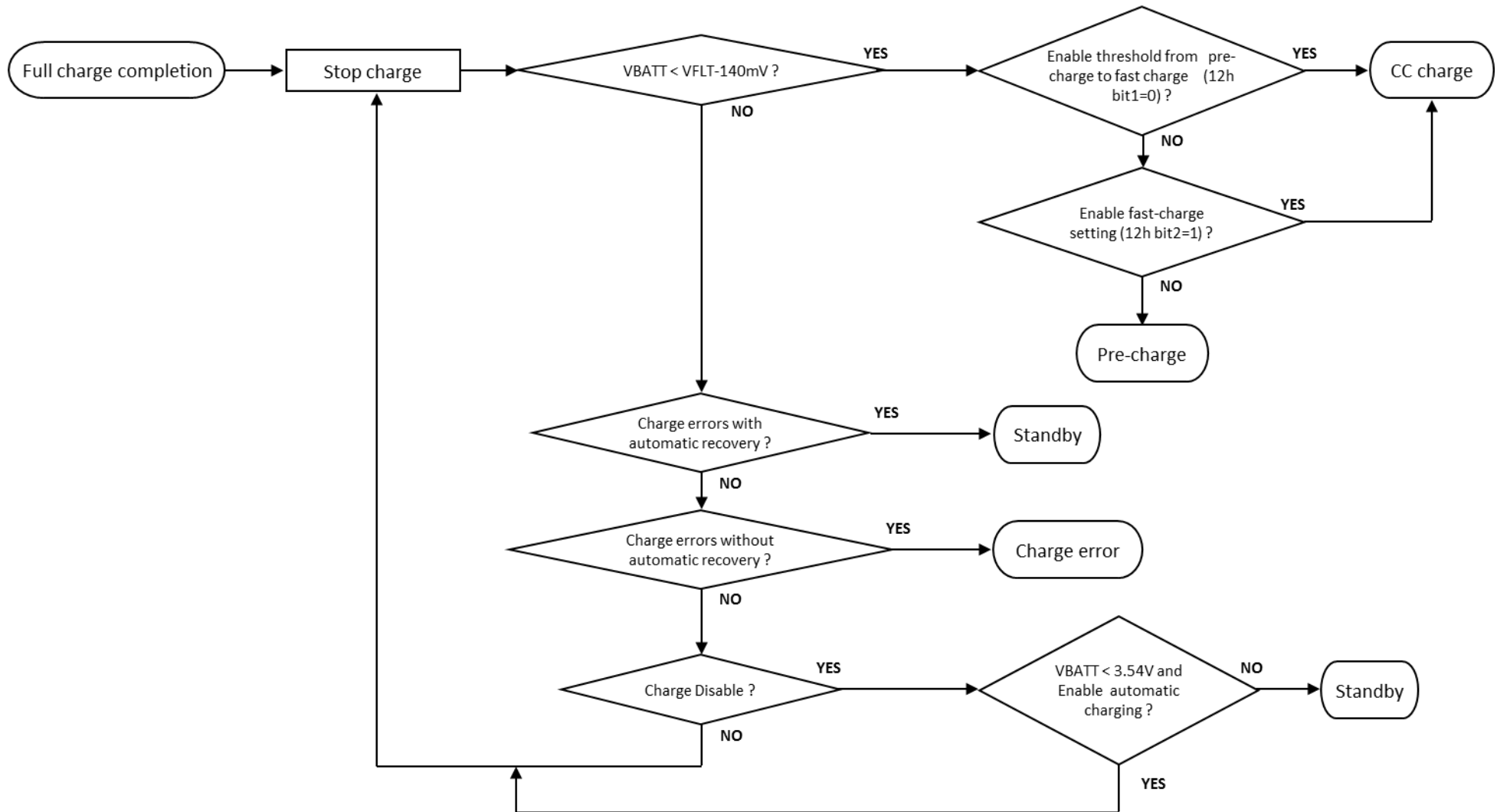


Figure 10-7 Flow chart: Full charge



<Unconnected battery detection>

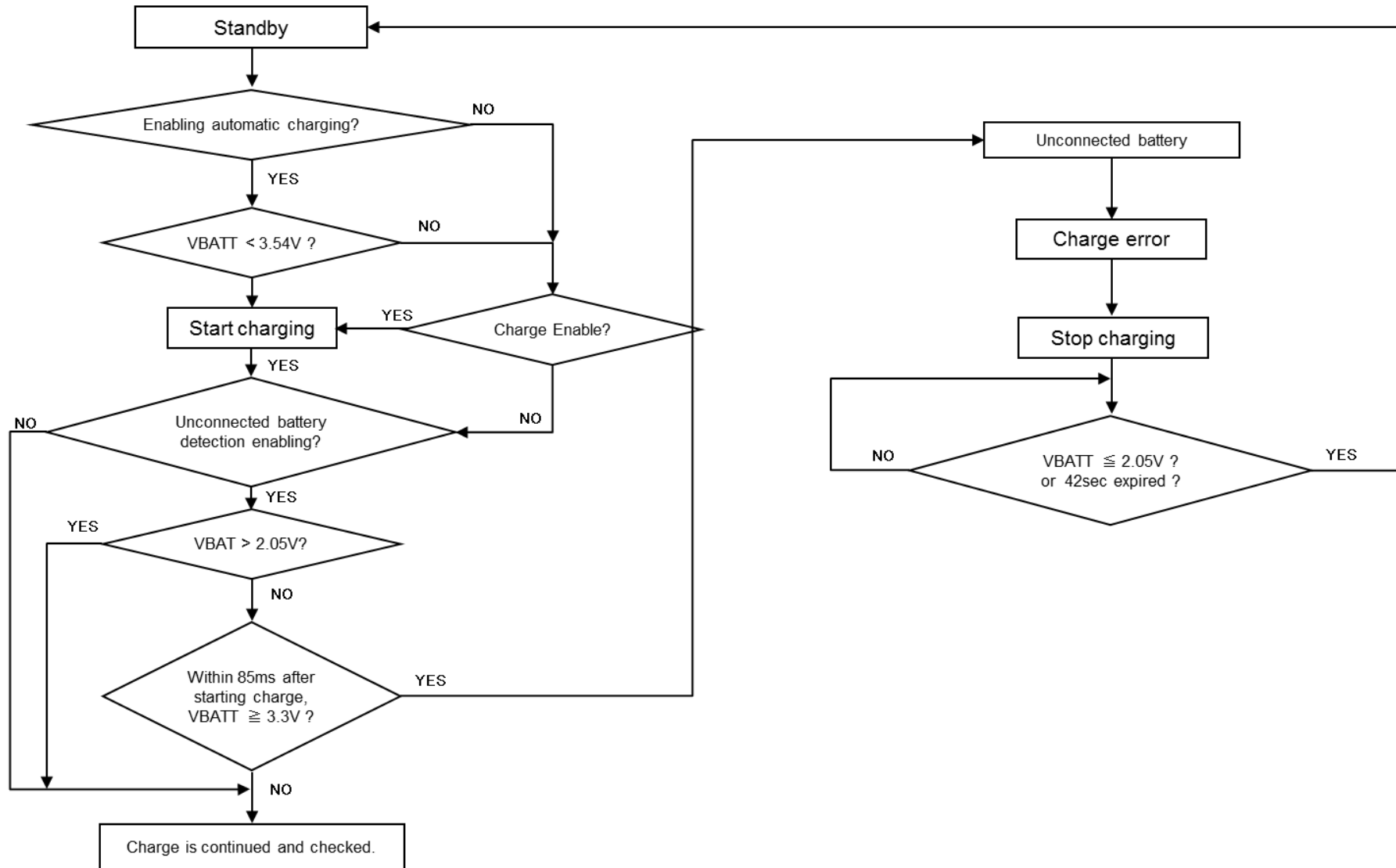


Figure 10-8 Flow chart: Unconnected battery detection

<OTG>

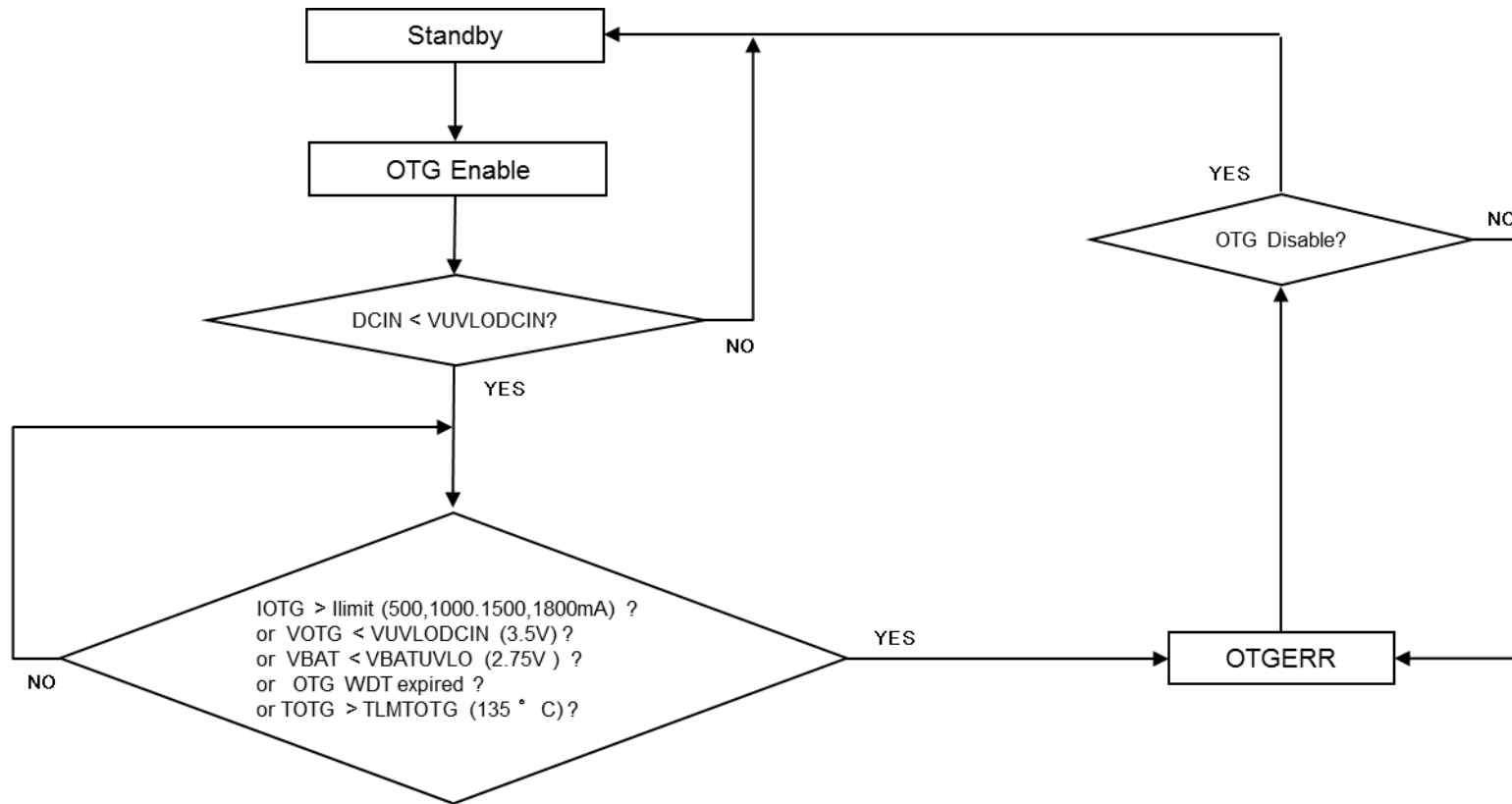
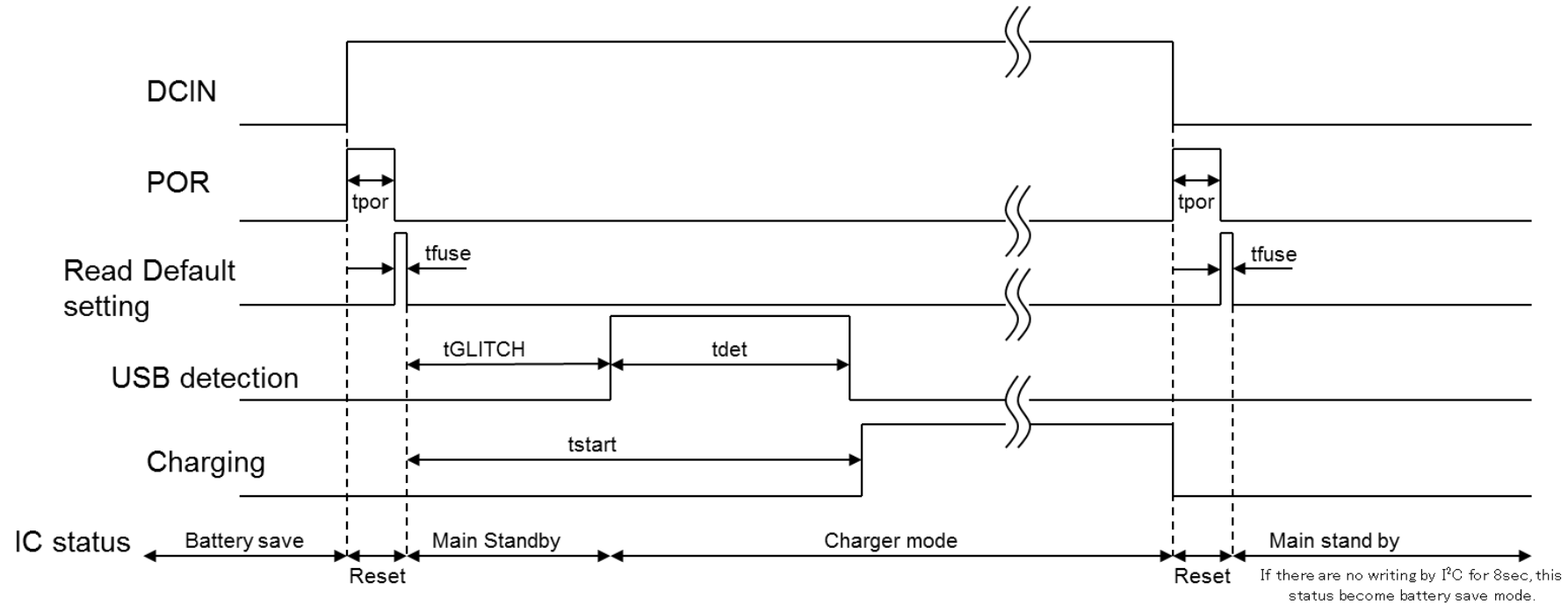


Figure 10-9 Flow chart: OTG

11. Timing chart

<DCIN ON / OFF>



| Symbol       | Contents                            | Time                            |
|--------------|-------------------------------------|---------------------------------|
| $t_{por}$    | DCIN~POR time                       | 20ms (Max)                      |
| $t_{fuse}$   | Read default setting                | 5 $\mu$ s (Max)                 |
| $t_{GLITCH}$ | Removal Chattering                  | 168ms (Max210ms)                |
| $t_{det}$    | USB detection time: No connect case | 470ms (Max)                     |
|              | USB detection time: SDP             | 95ms (Max)                      |
|              | USB detection time: CDP/DCP         | 164ms (Max)                     |
| $t_{start}$  | DCIN~start charging                 | $t_{dchat} + t_{det} + 1 \mu$ s |

Figure 11-1 Timing chart: DCIN ON / OFF

<Forced charge termination>

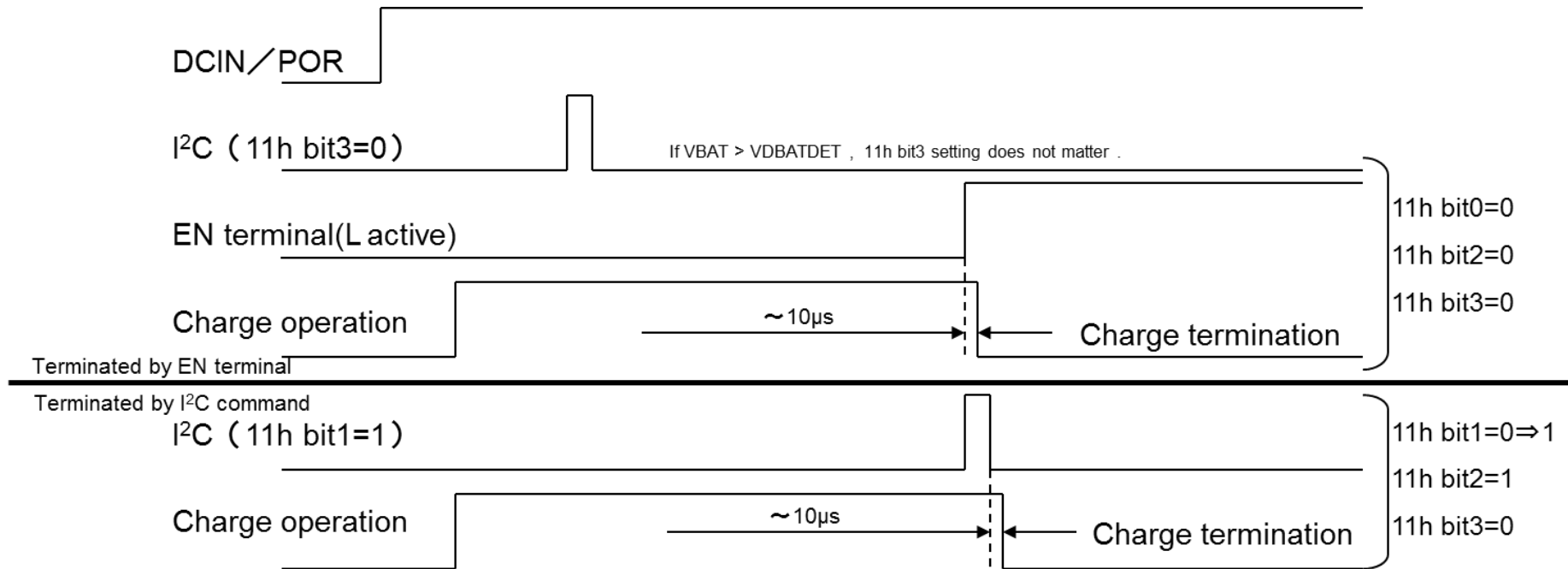


Figure 11-2 Timing chart: Forced charge termination

|                                   |                              |   |
|-----------------------------------|------------------------------|---|
| Auto charge control               | 11H,bit3="0"<br>11H,bit3="1" | Set charge disable, forced charge termination.<br>Set charge disable, charge operates if VBAT < VDBATDET(00H,bit7). [Initial value] |
| EN control polarity               | 11H,bit2="0"<br>11H,bit2="1" | Controlled by EN pin. [Initial value]<br>Controlled by I <sup>2</sup> C command.  |
| EN controlled by I <sup>2</sup> C | 11H,bit1="0"<br>11H,bit1="1" | Charge enable<br>Charge disable   |
| EN pin polarity select            | 11H,bit0="0"<br>11H,bit0="1" | L active (EN=L: Enable, H: Disable)<br>H active (EN=H: Enable, L: Disable)  |

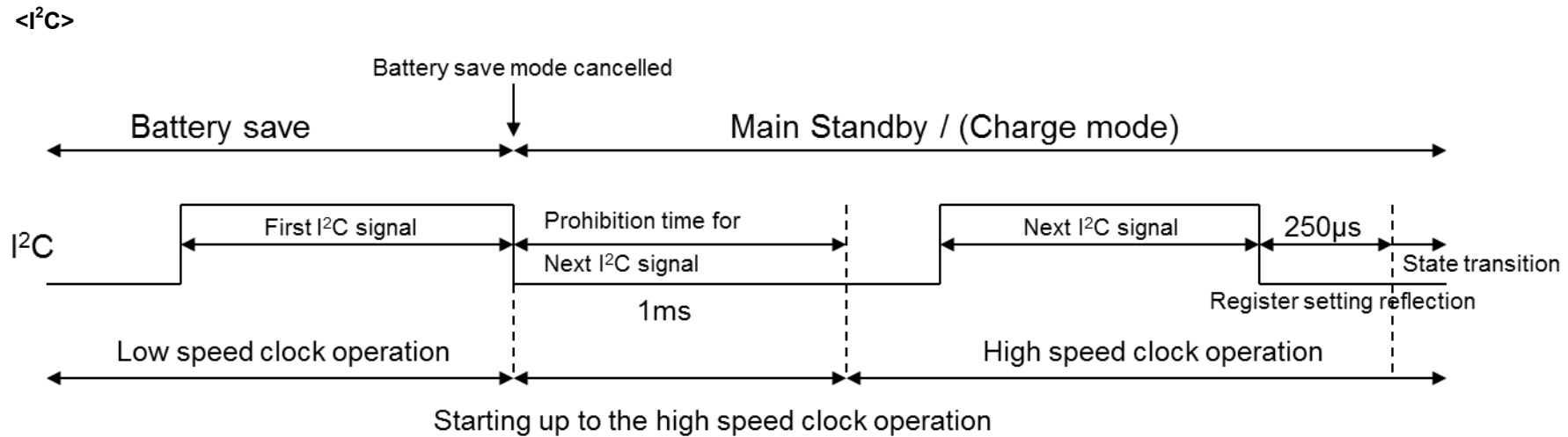


Figure 11-3 Timing chart: I<sup>2</sup>C

- When DCIN = UVLO and standby WDT is invalid, or OTG = Disable, the TC7710WBG becomes the battery save mode.
- If there is an I<sup>2</sup>C signal among the battery save mode, the TC7710WBG changes the mode to the standby mode.  
Wait time 1ms is necessary to write next I<sup>2</sup>C signal successively.
- If standby WDT is valid by command in the battery save mode, the TC7710WBG cannot resume the battery save mode.
- When the TC7710WBG is communicated by I<sup>2</sup>C in standby mode or charge mode, register setting is reflect soon, but state transition is occurred 250µs after that.  
If I<sup>2</sup>C command is set successively in 250µs, state transition is occurred 250µs after last communication.

## 12. Absolute Maximum Ratings

**Table 12-1 Absolute maximum ratings**

(Unless otherwise specified, Ta = 25°C)

| Characteristics                      | Symbol | Rating       | Unit | Remarks |
|--------------------------------------|--------|--------------|------|---------|
| Applied voltage of SW pin            | Vin1   | -0.3 to 6.5  | V    |         |
| Applied voltage of DCIN pin, MID pin | Vin2   | -1.5 to 10.0 | V    |         |
| Applied voltage of STAT pin          | Vin3   | -0.3 to 6.5  | V    |         |
| Applied voltage of other pins        | Vin4   | -0.3 to 6.5  | V    |         |
| Power dissipation 1 (*Note1)         | PDmax  | 1080         | mW   |         |
| Operating temperature (*Note2)       | Topr   | -40 to 85    | °C   |         |
| Junction temperature                 | Tj     | 150          | °C   |         |
| Storage temperature                  | Tstg   | -55 to 150   | °C   |         |

Note1: When Ta is 25°C or more, 16.67mW decreases per 1°C rise.

Note2: The operation range of actual use without any problems.

Note3: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

### 13. Electrical Characteristics

#### DC characteristics (1)

**Table 13-1 DC characteristics**

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^{\circ}C$ , all voltages are relative to GND.)

| Characteristics   | Symbol       | Test condition   | Min   | Typ.              | Max  | Unit        |
|---|--------------|--|-------|-------------------|------|-------------|
| <b>Input voltage</b>                                      | VDCIN        |  | +4.35 |                   | +6.5 | V           |
| <b>Input UVLO voltage</b>                                 | VUVLODCIN    | VDCIN rising   | 3.40  | 3.60              | 3.80 | V           |
|   |              | VDCIN falling  | 3.20  | 3.50              | 3.70 | V           |
| <b>Input OVLO voltage</b>                                 | VOVLODCIN    | VDCIN rising (no glitch filter)  | 6.20  | 6.50              | 6.90 | V           |
|   |              | VDCIN falling  | 6.10  | 6.30              | 6.60 | V           |
| <b>VMONI output voltage</b>                               | VVMONIRNG    | VUVLODCIN < VDCIN < VOVLODCIN,   |       | VDCIN-1.0         |      | V           |
| <b>VMONI output On-resistance</b>                         | RVMONI       |  |       | 1.7               |      | k $\Omega$  |
| <b>Current limit threshold accuracy</b>                   | VCLACC       | AC mode, VCL = 4.5V  | -4    |                   | +4   | %           |
| <b>Battery OVLO voltage</b>                               | VBOV         | $\Delta = 150mV$ or $200mV$  |       | VFLT+<br>$\Delta$ |      | V           |
| <b>Automatic shutdown threshold</b>                       | VASHDN       | VDCIN - VBATT,<br>VDCIN rising   | 60    | 130               | 200  | mV          |
|   |              | VDCIN - VBATT,<br>VDCIN falling  | 0     | 60                | 130  | mV          |
| <b>DCIN current (Active)</b>                              | IDCIN-ACTIVE | Charging, not including ICHG, Linear   |       | 1.6               |      | mA          |
|   |              | Charging, not including ICHG, PWM  |       | 14                |      | mA          |
| <b>Shutdown current</b>                                   | ISHDN        | Charge invalid, VDCIN = 5V, VBATT = 3.7V,<br>no load, DCIN $\geq$ UVLO, standby mode |       | 1.3               | 2.5  | mA          |
| <b>Battery shutdown current</b>                           | IAUXSHDN     | Current from battery<br>DCIN = OPEN, VBATT = 3.7V                                    |       | 38                | 67   | $\mu$ A     |
| <b>Leakage current</b>                                    | IDCINLK      | DCIN current when charge is invalid,<br>VDCIN = 1V, VBATT = 4.2V                     |       |                   | 2    | $\mu$ A     |
| <b>OTG current</b>  | IDDMOTG      | OTG valid, VBATT = 3.7V, no load   |       | 4                 |      | mA          |
| <b>Over temperature threshold, charge mode</b>            | TLIMITCHG    |  |       | 135               |      | $^{\circ}C$ |
| <b>Over temperature threshold hysteresis, charge mode</b> | THYSTCHG     |  |       | 20                |      | $^{\circ}C$ |
| <b>Over temperature threshold, OTG mode</b>               | TLIMITOTG    |  |       | 135               |      | $^{\circ}C$ |
| <b>Over temperature threshold hysteresis, OTG mode</b>    | THYSTOTG     |  |       | 20                |      | $^{\circ}C$ |

## DC characteristics (2) SW mode controller

Table 13-2 DC characteristic (continued)

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^\circ C$ , all voltages are relative to GND.)

| Characteristics   | Symbol | Test condition                 | Min | Typ. | Max | Unit |
|-------------------|--------|--------------------------------|-----|------|-----|------|
| FET on-resistance | RRDSON | High-side (DCIN to SW), Note 3 |     | 233  | 367 | mΩ   |
|                   |        | Low-side (SW to GND), Note 3   |     | 125  | 200 | mΩ   |
| Current limit     | ILIMIT | $V_{BATT} = 3.0V$              |     | 3    |     | A    |
| Duty cycle        | D.C.   | Maximum                        |     | 100  |     | %    |
|                   |        | Minimum                        |     | 0    |     | %    |

## DC characteristics (3) Battery charger

Table 13-3 DC characteristics (continued)

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^\circ C$ , all voltages are relative to GND.)

| Characteristics   | Symbol      | Test condition  | Min  | Typ. | Max  | Unit |
|---|-------------|---|------|------|------|------|
| Trickle charge to Pre-charge voltage threshold                      | VTRICKLECHG |   | 1.9  | 2.05 | 2.2  | V    |
| Unconnected battery voltage threshold                               | VBATMIS     |   | 3.15 | 3.3  | 3.45 | V    |
| Trickle charge current  | ITRICKLECHG | $V_{BATT} = 1.7V$   | 30   | 50   | 80   | mA   |
| Dead battery voltage threshold                                      | VBATDEAD    | Programmable (2 settings): 3.47V, 3.54V   | -4   |      | 4    | %    |
| Pre-charge to Fast charge voltage threshold                         | VPRECHG     | Programmable $V_{PRECHG} = 2.6$ to $3.3$ V (8steps)                               | -3.5 |      | 3.5  | %    |
| USB1 input current limit  | IUSB1LMT    | $T_a = 0$ to $70^\circ C$ , $I_{USB1LMT} = 90mA$ , Note 2, $V_{MONI}$ off         | 60   | 80   | 100  | mA   |
| USB5 input current limit  | IUSB5LMT    | $T_a = 0$ to $70^\circ C$ , $I_{USB5LMT} = 475mA$ ,                               | 400  | 460  | 500  | mA   |
| AC input current limit (programmable 300mA to 2000mA, 18steps)      | IACLMT      | $T_a = 0$ to $70^\circ C$ , $I_{ACLMT} = 500mA$                                   | -100 |      | 55   | mA   |
| Constant current sense voltage                                      | VSENSE      | $I_{FCHG} = 1000mA$   |      | 68   |      | mV   |
| Pre-charge current (programmable 50mA to 200mA, 50mA/step)          | IPRECHG     | $T_a = 0$ to $70^\circ C$ , $I_{PRECHG} = 100mA$ , Note 1                         | -30  |      | 30   | mA   |
| Fast charge current (programmable 300mA to 2000mA, 18steps)         | IFCHG       | $T_a = 0$ to $70^\circ C$ , $R_{SENSE} = 68m\Omega$ , $I_{FCHG} = 500mA$ , Note 1 | -50  |      | 50   | mA   |
| Charge termination current (Programmable 100mA to 200mA, 50mA/step) | ITERM       | $T_a = 0$ to $70^\circ C$ , $R_{SENSE} = 68m\Omega$ , $I_{TERM} = 100mA$          | -30  |      | 30   | mA   |
| Charge termination current (Programmable 100mA to 200mA, 50mA/step) | ITERM       | $T_a = 0$ to $70^\circ C$ , $R_{SENSE} = 68m\Omega$ , $I_{TERM} = 150mA, 200mA$   | -30  |      | 30   | %    |
| Float voltage (Programmable 3.46V to 4.72V, 10mV/step)              | VFLT        | $T_a = 0$ to $70^\circ C$ , $V_{FLT} = 4.0V$ to $4.42V$                           | -1   |      | 1    | %    |
| Automatic re-charge threshold voltage                               | VRECH       |   | 70   | 140  | 190  | mV   |



## DC characteristics (4) Thermal monitor (Factory programmable option)

Table 13-4 DC characteristics (continued)

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^\circ C$ , all voltages are relative to GND.)

| Characteristics   | Symbol  | Test condition  | Min   | Typ.  | Max   | Unit    |
|---|---------|---|-------|-------|-------|---------|
| High temperature trip point<br>(Programmable 509mV to 726mV, 4steps)  | VHOT    | V <sub>THERM</sub> falling,<br>V <sub>HOT</sub> = 0.726V, $T_a = 0$ to $70^\circ C$ | 675   | 726   | 776   | mV      |
| Low temperature trip point<br>(Programmable 1.399V to 1.654V, 4steps) | VCOLD   | V <sub>THERM</sub> rising,<br>V <sub>COLD</sub> = 1.491V, $T_a = 0$ to $70^\circ C$ | 1.437 | 1.491 | 1.543 | V       |
| Current source for NTC<br>thermistor                                  | INTC    | 10k $\Omega$ NTC, $T_a = 0$ to $70^\circ C$   | 180   | 200   | 220   | $\mu A$ |
|   |         | 25k $\Omega$ NTC  | 72    | 80    | 88    | $\mu A$ |
|   |         | 50k $\Omega$ NTC  | 36    | 40    | 44    | $\mu A$ |
|   |         | 100k $\Omega$ NTC   | 18    | 20    | 22    | $\mu A$ |
| Current source hysteresis for<br>NTC thermistor                       | INTCHYS | High temperature hysteresis,<br>INTC = 200 $\mu A$                                  | 160   | 180   | 198   | $\mu A$ |
|   |         | Low temperature hysteresis,<br>INTC = 200 $\mu A$                                   | 198   | 220   | 242   | $\mu A$ |

## DC characteristics (5) Logic inputs / outputs

Table 13-5 DC characteristics (continued)

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^\circ C$ , all voltages are relative to GND.)

| Characteristics                           | Symbol                 | Test condition                         | Min | Typ. | Max | Unit    |
|---|------------------------|--|-----|------|-----|---------|
| Input "L" level                           | V <sub>IL</sub>        |  |     |      | 600 | mV      |
| Input "H" level                           | V <sub>IH</sub>        |  | 1.4 |      |     | V       |
| SDA / STAT output "L" level               | V <sub>OL</sub>        | I <sub>SINK</sub> = 3mA                |     |      | 300 | mV      |
| STAT leakage current                      | I <sub>STATLK</sub>    |  |     |      | 1   | $\mu A$ |
| EN input bias current                     | I <sub>ENBIAS</sub>    |  |     |      | 1   | $\mu A$ |
| ILIM_OTG logic level voltage<br>threshold | V <sub>ILIMOTG</sub>   | Input logic low-to-high state          |     | 0.9  |     | V       |
| ILIM_OTG input bias current               | I <sub>ILIMOTGBS</sub> | Input logic low                        |     | < 10 |     | nA      |
|   |                        | Input logic high, pull-up voltage 3.3V |     | +5.5 | +8  | $\mu A$ |

## DC characteristics (6) USB OTG power

Table 13-6 DC characteristics (continued)

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^\circ C$ , all voltages are relative to GND.)

| Characteristics           | Symbol     | Test condition  | Min  | Typ. | Max  | Unit |
|---------------------------|------------|---|------|------|------|------|
| Output voltage (DCIN pin) | VOTG       | $V_{BATT} = 3.6V$ , programmable 4steps, 5.0V output setting                        | 4.75 | 5.0  | 5.25 | V    |
| UVLO battery voltage      | VBATUVLO   | OTG operation (refer to register 04H), 2.75V setting                                | 2.63 | 2.75 | 2.87 | V    |
| UVLO hysteresis           | VBATUVLOHY | OTG operation   | 110  | 170  | 230  | mV   |
| OTG battery current range | IOTG       | $V_{BATT} = 3.6V$ , current from battery, programmable 4steps, CCI4-0=500mA, Note 4 | 400  | 500  | 600  | mA   |
|                           |            | CCI4-0=1000mA   | 800  | 1000 | 1200 |      |
|                           |            | CCI4-0=1500mA   | 1200 | 1500 | 1800 |      |
|                           |            | CCI4-0=1800mA   | 1440 | 1800 | 2160 |      |

## DC characteristics (7) Automatic power source detection (DP / DM) Note 5

Table 13-7 DC characteristics (continued)

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^\circ C$ , all voltages are relative to GND.)

| Characteristics                             | Symbol   | Test condition | Min   | Typ. | Max   | Unit       |
|---|----------|----------------|-------|------|-------|------------|
| Data line leakage voltage                   | VDAT_LKG |                | 0     |      | 3.6   | V          |
| Data detection voltage                      | VDAT_REF |                | 0.25  | 0.33 | 0.40  | V          |
| D+ source voltage                           | VDP_SRC  |                | 0.50  | 0.60 | 0.70  | V          |
| D- source voltage                           | VDM_SRC  |                | 0.50  | 0.60 | 0.70  | V          |
| D+ pull-up voltage                          | VDP_UP   |                | 3.0   | 3.3  | 3.6   | V          |
| Logic threshold                             | VLGC     |                | 0.8   | 1.2  | 2.0   | V          |
| D+ sink current                             | IDP_SINK |                | 25    | 100  | 175   | $\mu A$    |
| D- sink current                             | IDM_SINK |                | 25    | 100  | 175   | $\mu A$    |
| Current source for data connected detection | IDP_SRC  |                | 7     | 10   | 13    | $\mu A$    |
| Data line leakage resistance                | RDAT_LKG |                | 300   |      |       | k $\Omega$ |
| D- pull-down resistance                     | RDM_DOWN |                | 14.25 | 20.0 | 24.80 | k $\Omega$ |
| D+ pull-up resistance                       | RDP_UP   |                | 900   | 1200 | 1575  | $\Omega$   |

## AC characteristics (1) Oscillator

Table 13-8 AC characteristics

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^\circ C$ , all voltages are relative to GND.)

| Characteristics                                  | Symbol  | Test condition            | Min  | Typ. | Max  | Unit |
|--|---------|---------------------------|------|------|------|------|
| Oscillator frequency 1, Timer frequency          | fOSC    | $T_a = 0$ to $70^\circ C$ | 2.40 | 3.0  | 3.60 | MHz  |
| Start-up time                                    | tSTART  |                           |      |      | 20   | ms   |
| Oscillator frequency 2, Start-up timer frequency | fTM     | $T_a = 0$ to $70^\circ C$ |      | 85   |      | kHz  |
| Pre-charge time out                              | tPCTOFC | Safety timer              | 29   | 36   | 43   | min  |
| Charge completion time out                       | tCTOFC  | Safety timer              | 204  | 240  | 276  | min  |
| Charge watchdog timer                            | tCWD    |                           | 33.6 | 42   | 50.4 | sec  |
| OTG power watchdog timer                         | tOTGWD  |                           | 33.6 | 42   | 50.4 | sec  |
| Standby watchdog timer                           | tSTBYWD | No charging, no OTG power | 21   | 42   | 63   | sec  |
| Unconnected battery timer                        | tBATMIS |                           | 65   | 86   | 105  | ms   |
| Device glitch filter                             | tGLITCH | Enabled                   | 130  | 168  | 210  | ms   |

## AC characteristics (2) Power source detection

Table 13-9 AC characteristics (continued)

(Unless otherwise specified,  $V_{DCIN} = 5.0V$ ,  $V_{FLT} = 4.2V$ ,  $V_{BATT} = 3.7V$ ,  $T_a = -30$  to  $85^\circ C$ , all voltages are relative to GND.)

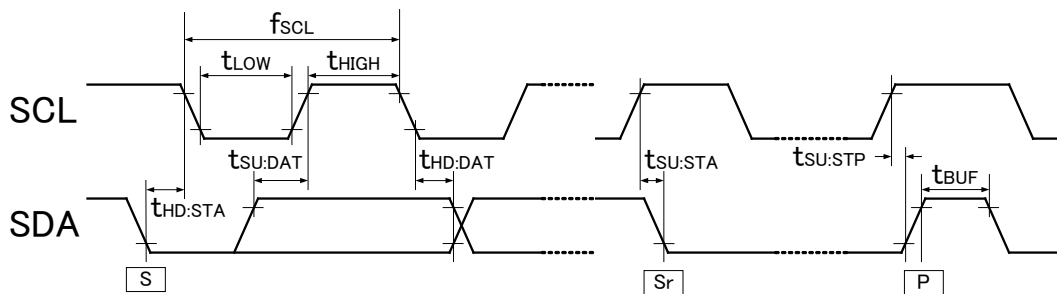
| Characteristics                   | Symbol       | Test condition | Min | Typ. | Max | Unit |
|-----------------------------------|--------------|----------------|-----|------|-----|------|
| Data connected detection debounce | tDCD_DBNC    | Note 3, 5      | 10  |      |     | ms   |
| Data connected detection time out | tDCD_TIMEOUT | Note 3, 5      | 300 |      |     | ms   |
| DP source on time                 | tVDPSRC_ON   | Note 3, 5      | 40  |      |     | ms   |
| DM source on time                 | tVDMSRC_ON   | Note 3, 5      | 40  |      |     | ms   |

**AC characteristics (3) I<sup>2</sup>C interface @ 400kHz**

**Table 13-10 AC characteristics (continued)**

(Unless otherwise specified, V<sub>D</sub>CIN = 5.0V, V<sub>F</sub>LT = 4.2V, V<sub>B</sub>BATT = 3.7V, T<sub>a</sub> = -30 to 85°C, all voltages are relative to GND.)

| Characteristics                                   | Symbol              | Test condition    | Min      | Typ. | Max | Unit |
|---|---------------------|-------------------|----------|------|-----|------|
| SCL clock frequency                               | f <sub>SCL</sub>    |                   | 0        |      | 400 | kHz  |
| SCL clock low period                              | t <sub>LOW</sub>    |                   | 1.3      |      |     | μs   |
| SCL clock high period                             | t <sub>HIGH</sub>   |                   | 0.6      |      |     | μs   |
| Bus free time (Stop condition to Start condition) | t <sub>BUF</sub>    | Note 6            | 1.3      |      |     | μs   |
| START condition setup time                        | t <sub>SU:STA</sub> |                   | 0.6      |      |     | μs   |
| START condition hold time                         | t <sub>HD:STA</sub> |                   | 0.6      |      |     | μs   |
| STOP condition setup time                         | t <sub>SU:STO</sub> |                   | 0.6      |      |     | μs   |
| SCL / SDA rising time                             | t <sub>R</sub>      | Note 6            | 20+0.1Cb |      | 300 | ns   |
| SCL / SDA falling time                            | t <sub>F</sub>      | Note 6            | 20+0.1Cb |      | 300 | ns   |
| Data in setup time                                | t <sub>SU:DAT</sub> |                   | 100      |      |     | ns   |
| Data in hold time                                 | t <sub>HD:DAT</sub> |                   | 0        |      | 0.9 | μs   |
| Noise filter                                      | TI                  | Noise suppression |          | 80   |     | ns   |



**Figure 13-1 I<sup>2</sup>C interface**

Note 1 : Input current limit I<sub>LIM</sub> is prior to I<sub>P</sub>RECHG ,I<sub>F</sub>CHG.

Note 2 : IC is not used as a battery protection.

Note 3 : Design and characteristics are guaranteed. Not 100% test.

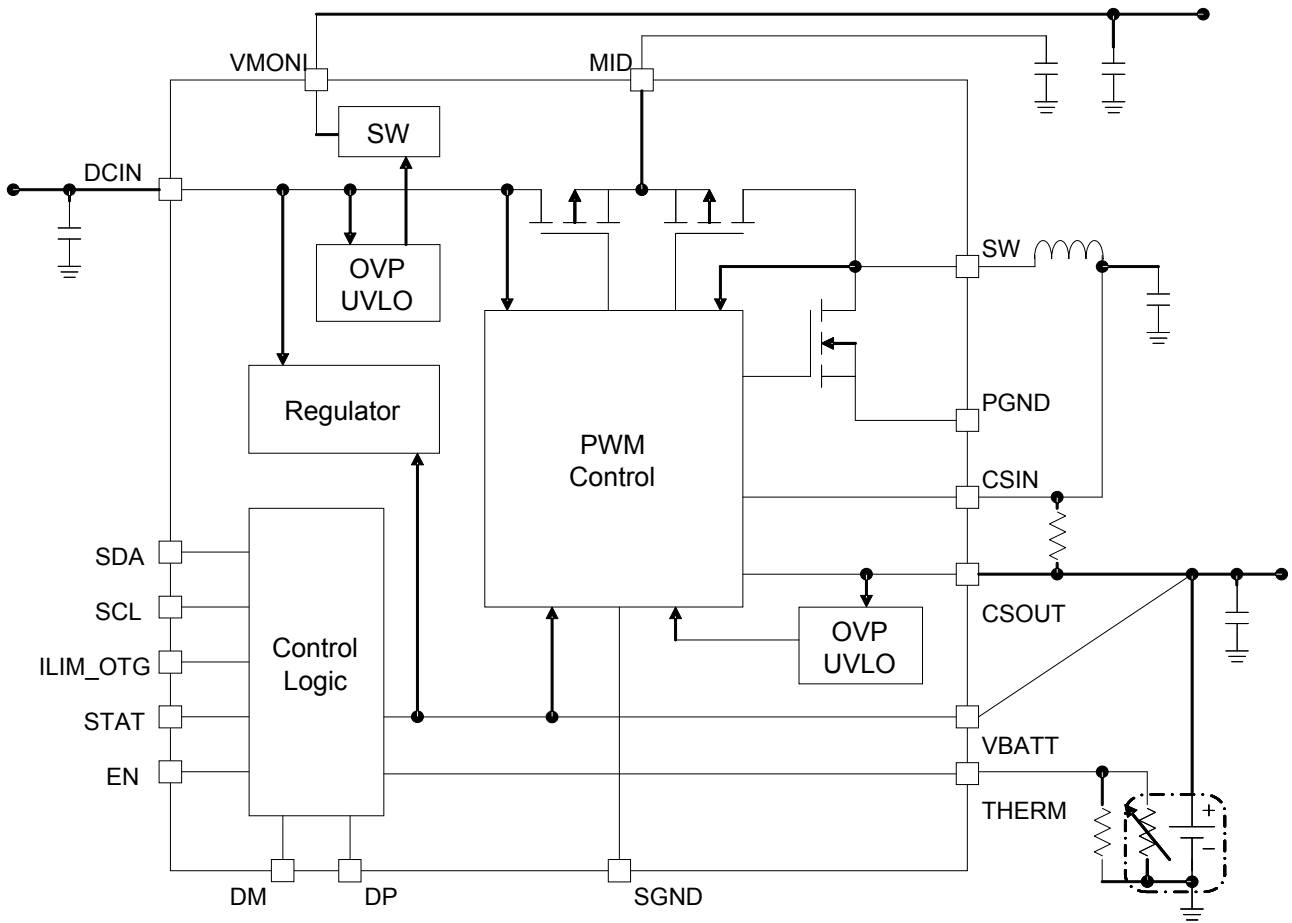
Note 4 : OTG power path is shut off after 168ms (glitch filter period) since the selected OTG current limit is reached.

To re-start OTG power path, set OTG mode invalid, and then set it valid.

Note 5 : Refer to Battery Charging Specification Rev1.2.

Note 6 : Guaranteed by design.

**14. Application Circuit**

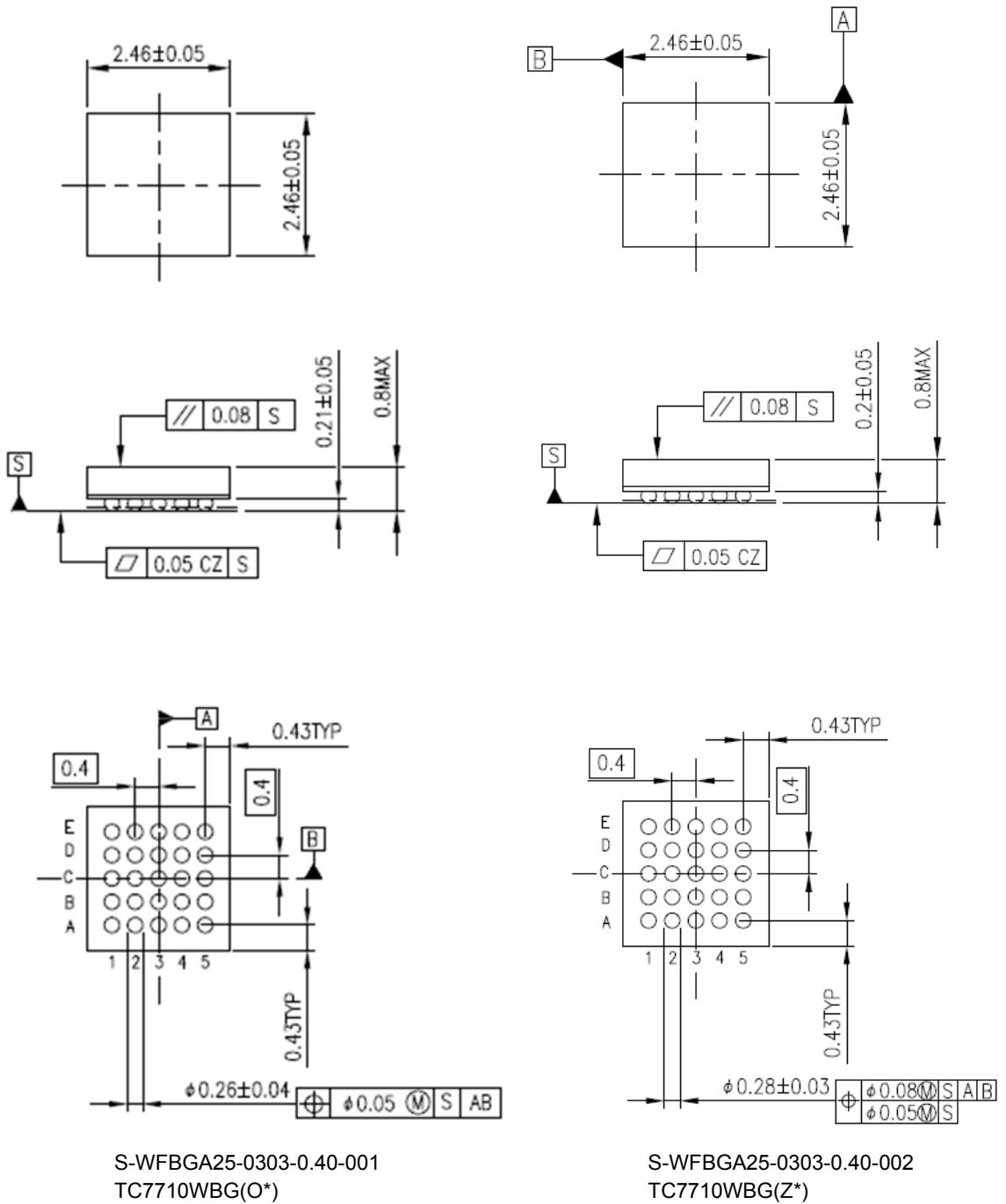


**Figure 14-1 Application circuit**

**15. Outline drawing**

**15.1 Package Dimensions**

Unit: mm



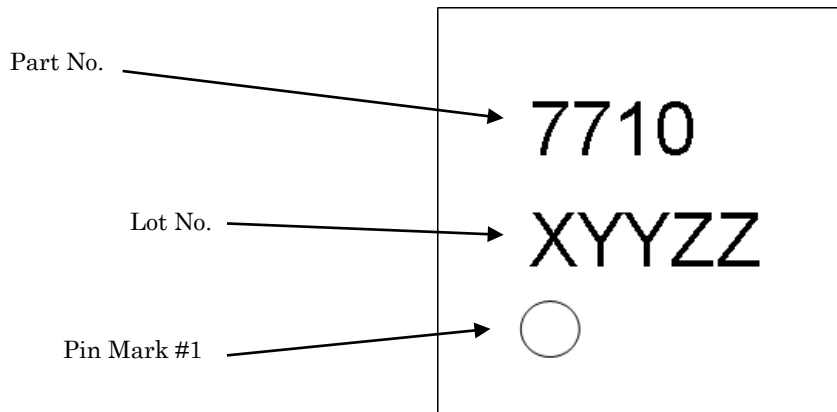
S-WFBGA25-0303-0.40-001  
TC7710WBG(O\*)

S-WFBGA25-0303-0.40-002  
TC7710WBG(Z\*)

Weight: 0.009 g (Typ.)

15.2 Marking

TC7710WBG(O\*) Marking



TC7710WBG(O\*) Lot No.:

X YY ZZ  
 (1) (2) (3)

(1) Manufactured year code Annual code expressed as the last digit of year

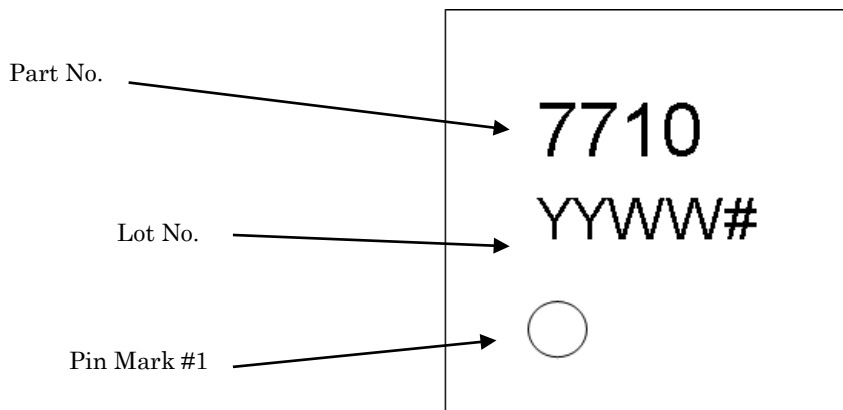
Example

|      |      |      |      |      |      |
|------|------|------|------|------|------|
| Year | 2009 | 2010 | 2011 | 2012 | 2013 |
| Code | 9    | 0    | 1    | 2    | 3    |

(2) Manufactured week code Weekly code as the first Thursday of January being determined the first week and accordingly reaches 52nd or 53th week in a year.

(3) Our control number

TC7710WBG(Z\*) Marking



TC7710WBG(Z\*) Lot No.:

YY WW #  
 (1) (2) (3)

(1) Manufactured year code Annual code expressed as the last digit of year

Example

|      |      |      |      |      |      |
|------|------|------|------|------|------|
| Year | 2009 | 2010 | 2011 | 2012 | 2013 |
| Code | 09   | 10   | 11   | 12   | 13   |

(2) Manufactured week code Weekly code as the first week of January being determined 01 and accordingly reaches 52nd or 53th week in a year.

(3) Our control number

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